PY32F403-C Datasheet

32-bit ARM® Cortex®-M4F Microcontroller

Puya Semiconductor (Shanghai) Co., Ltd.

Features

- Core
  - 32-bit ARM® Cortex®-M4F CPU with FPU and DSP instructions
  - Frequency up to 144 MHz
- Memories
  - Up to 384 KB Flash memory
  - Up to 64 KB SRAM
- Reset and supply management
  - 1.8 to 3.6 V
  - Power-on/power-down reset (POR/PDR)
  - Programmable voltage detector (PVD)
- Clocks
  - 8 MHz high-speed internal RC oscillator (HSI8)
  - 48 MHz high-speed internal RC oscillator for dedicated use (HSI48)
  - 40 kHz low-speed internal RC oscillator (LSI)
  - 4 to 32 MHz high-speed external crystal oscillator (HSE)
  - 32.768 kHz low-speed external crystal oscillator (LSE)
  - PLL supports CPU up to 144 MHz
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC and backup registers
- 3 x 12 bit ADC
  - 1 µs A/D converters (up to 20 channels)
  - Conversion range: 0 to V_{CCA}
  - Supports sampling time and resolution configuration
  - Supports single, continuous, scan and discontinuous modes
  - Temperature sensor
  - Voltage sensor
  - Supports Timer and EXTI triggering
- 2 x 12-bit D/A converters
  - Output range: 0 to V_{REF+}
  - Independent output channel
  - Supports Timer and EXTI triggering
- 12-channel DMA controller
  - Supported peripherals: Timer, ADC, DAC, UART, I^2C, I^2S, SPI and SDIO
- Up to 80 fast I/Os:
  - All mappable on 16 external interrupt vectors
  - Some ports support 5 V-tolerant
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- Up to 17 timers
  - 2 x 16-bit advanced-control timers, having 4-channel PWM timers with dead-time generation and emergency stop
  - 10 x 16-bit general-purpose timers with up to 4 independent channels for input capture/output comparison, the general purpose timers also support encoder interfaces using two inputs of quadrature decoders
  - 2 x 16-bit basic timers to drive the DAC
  - 2 x watchdog timers (Independent & Window)
  - SysTick timer: a 24-bit downcounter
- Up to 13 communication interfaces
  - Up to 5 USARTs
  - Up to 2 x I^2C interfaces
  - Up to 3 SPIs
  - ESMC interface
  - CANFD interface
  - USB 2.0 full speed interface
  - SDIO interface
- 96-bit unique ID (UID)
- Packages: LQFP100, LQFP64, QFN64, LQFP48, QFN48 and QFN32 (4*4)

Content

1. Introduction

The PY32F403-C microcontrollers incorporate the high-performance ARM® 32-bit Cortex®-M4F core operating at up to 144 MHz frequency, embedded memories with up to 384 KB Flash and 64 KB SRAM, available in multiple package options. The device integrates multi-channel I^2C, SPI, USART and other communication peripherals. It has three 12-bit ADCs, two DACs, 17 timers, an USB 2.0 and a CANFD.

The PY32F403-C microcontrollers operate across a temperature range of -40 to 105 °C and a standard voltage range is from 1.8 to 3.6 V. They provides Sleep, Stop and Standby low power operating modes, which can meet different low-power applications.

These features make the PY32F403-C microcontrollers suitable for a wide range of applications such as controllers, portable devices, PC peripherals, gaming and GPS platforms, as well as industrial applications.

Table 1-1 PY32F403-C series LQFP100/LQFP64/QFN64/LQFP48 product features and peripheral counts

Peripherals		PY32F403V1DT7-C	PY32F403R1DT7-C	PY32F403R1DU7-C	PY32F403V1DT7-C
Flash (KB)		384	384	384	384
SRAM (KB)		64	64	64	64
Timers	General-purpose timers	10			
	Advanced-control timer	2			
	SysTick	1			
	Basic timers	2			
	Watchdog	2			
Comm. interfaces	USART	5	5	5	3
	I^2C	2	2	2	2
	SPI	3	3	3	3
	I^2S	3	3	3	3
	CANFD	1	1	1	1
	USBD	1			
	SDIO	1	1	1	-
DMA		12ch			
RTC		Yes			
GPIO		80	51	51	37
ESMC		1			
EXTI		16			
ADC (external + internal)		3 (16+4)	3 (16+4)	3 (16+4)	3 (10+4)
DAC (channels)		2(2)			
Operating voltage		1.8 ~ 3.6 V			
Max. CPU frequency		144 MHz			
Operating temperature		-40 ~ 105 ℃			
Packages		LQFP100	LQFP64	QFN64	LQFP48

Table 1-2 PY32F403-C series LQFP48/QFN48/QFN32 product features and peripheral counts

Peripherals		PY32F403C1CT7-C	PY32F403C1CU7-C	PY32F403K1CU7-C	PY32F403K1BU7-C
Flash (KB)		256	256	256	128
SRAM (KB)		64	64	64	32
Timers	General-purpose timers	10			
	Advanced-control timer	2			
	SysTick	1			
	Basic timers	2			
	Watchdog	2			
Comm. interfaces	USART	3	2	2	2
	I^2C	2	1	1	1
	SPI	3	3	2	2
	I^2S	3	3	2	2
	CANFD	1	1	1	1
	USBD	1			
	SDIO	-	-	-	-
DMA		12ch			
RTC		Yes			
GPIO		37	41	26	26
ESMC		1			
EXTI		16			
ADC (external + internal)		3 (10+4)	3 (11+4)	3 (10+4)	3 (10+4)
DAC (channels)		2(2)			
Operating voltage		1.8 ~ 3.6 V			
Max. CPU frequency		144 MHz			
Operating temperature		- 40 ~ 105 ℃			
Packages		LQFP48	QFN48	QFN32	

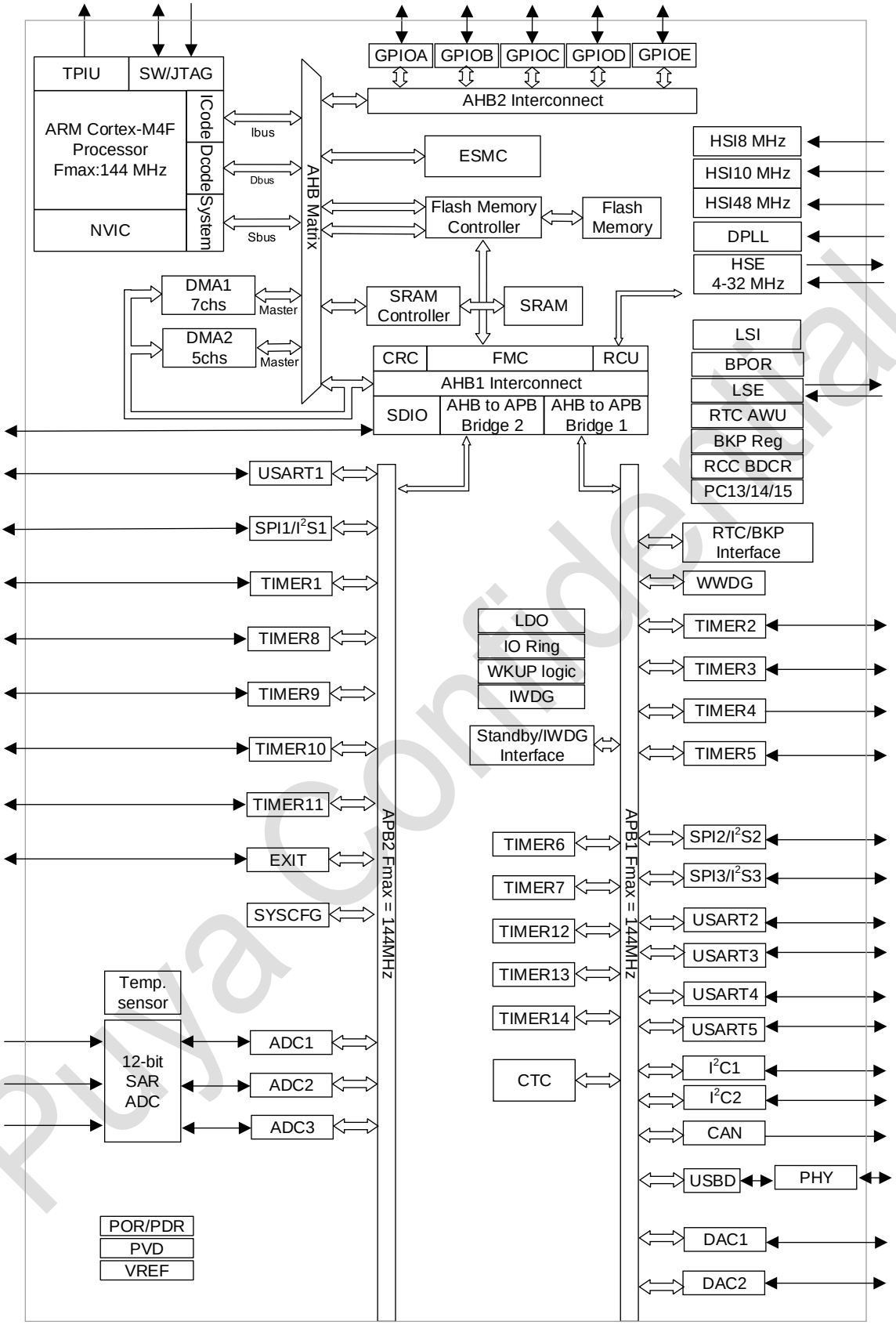


Figure 1-1 System block diagram

2. Functional overview

2.1. ARM® Cortex®-M4F core

ARM® 's Cortex®-M4F with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8-bit and 16-bit devices, supporting DSP instructions and FPU floating-point operations. The processor supports a set of DSP instructions, which allow efficient signal processing and complex algorithm execution. Its single-precision FPU (floating-point unit) speeds up software development by using metalanguage development tools, while avoiding saturation. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts. It is compatible with all Arm tools and software.

32-bit ARM® Cortex®-M4F Microcontroller

- Supports 144 MHz operating frequency
- Single cycle multiplier and hardware divider
- Integrated DSP instructions
- Nested vectored interrupt controller (NVIC)
- 24-bit Sys Tick timer

The ARM® Cortex®-M4F processor is based on the ARMv7-M architecture and supports Thumb and Thumb-2 instruction sets.

- The internal bus matrix connects the I-Code bus, D-Code bus, system bus, private peripheral bus (PPB) and advanced high-performance bus - access port (AHB-AP)
- Nested vectored interrupt controller (NVIC)
- Flash patch and breakpoint (FPB)
- Data watchpoint and trace (DWT)
- Instrumentation trace macrocell (ITM)
- Serial wire JTAG debug port (SWJ-DP)
- Trace port interface unit (TPIU)
- Floating point unit (FPU)
- Memory protection unit (MPU)

2.2. Memories

Embedded SRAM is accessed by byte (8 bits), half-word (16 bits) or word (32 bits).

The Flash memory is composed of two distinct physical areas:

- The Main flash area consists of application and user data
- 24 KB of Information area:
  - Option bytes
  - UID bytes

— System memory

The protection of Main flash area includes the following mechanisms:

- Read protection (RDP) blocks external access.
- Write protection (WRP) prevents unintended writes (caused by confusion of program). The minimum protection unit for write protection is 8 KB.
- Option byte write protection is a special design for unlock.

2.3. Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4GB of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and act. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed. The MPU is optional and can be bypassed for applications that do not need it.

2.4. Flash accelerator (ACC)

To release the processor full performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the flash memory. Based on the CoreMark benchmark, the performance achieved thanks to the accelerator is equivalent to 0 wait state program execution from the flash memory at a CPU frequency up to 144 MHz.

- ICODE can prefetch instructions
- The instruction cache has 64 branches and the data bit width is 128 bits
- The data cache has 16 branches, and the data bit width is 128 bits

2.5. Boot modes

At startup, the BOOT0 and nBOOT pin are used to select one of the three boot options in the following table:

Table 2-1 Boot configuration

Boot modes		Mode
BOOT1 Pin	BOOT0 pin	
X	0	Boot from Main flash
0	1	Boot from System memory
1	1	Boot from SRAM

The Boot loader is located in the system memory and is used to reprogram the Flash memory by using USART or USB interface.

2.6. Backup Register (BKP)

Backup registers are 42 16-bit registers used to store 84 bytes of user application data. This module is in the backup domain. When the V_{CC} power is off, they are still powered by V_{BAT}. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode.

- Supports 84-byte data backup register
- Status/control register for managing anti-intrusion detection and having interrupt function
- A check register used to store the RTC check value.
- Output an RTC calibration clock, an RTC alarm pulse or a second pulse on the PC13 pin (when this pin is not used for intrusion detection)

2.7. Clock management

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. After the program is operating the system clock frequency and system clock source can be reconfigured. The frequency clocks that can be selected are:

- An 8 MHz internal high-precision HSI8 clock
- A 48 MHz internal high-precision HSI48 clock
- A 40 kHz configurable internal LSI clock
- A 4 to 32 MHz HSE clock, and used to enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, and software configures the HSI frequency. Simultaneously, CPU NMI interrupt is generated.
- A 32.768 kHz LSE clock
- PLL clock has HSI and HSE sources. If the HSE source is selected, when CSS is enabled and CSS fails, disable PLL and HSE, and the system clock is automatically switched to HSI.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The maximum frequency of the AHB and the APB domains is 144 MHz.

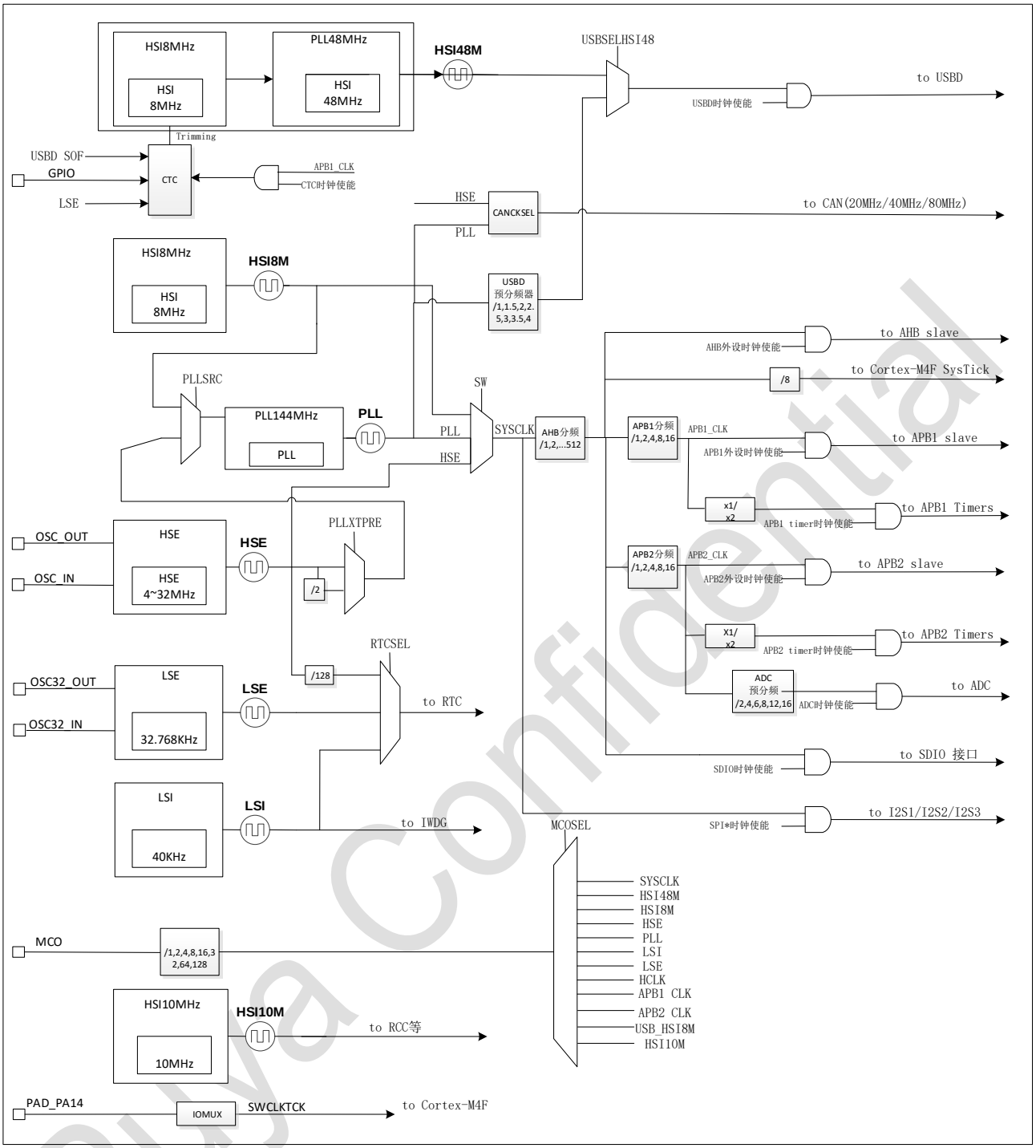


Figure 2-1 System clock structure diagram

2.8. Power management

2.8.1. Power block diagram

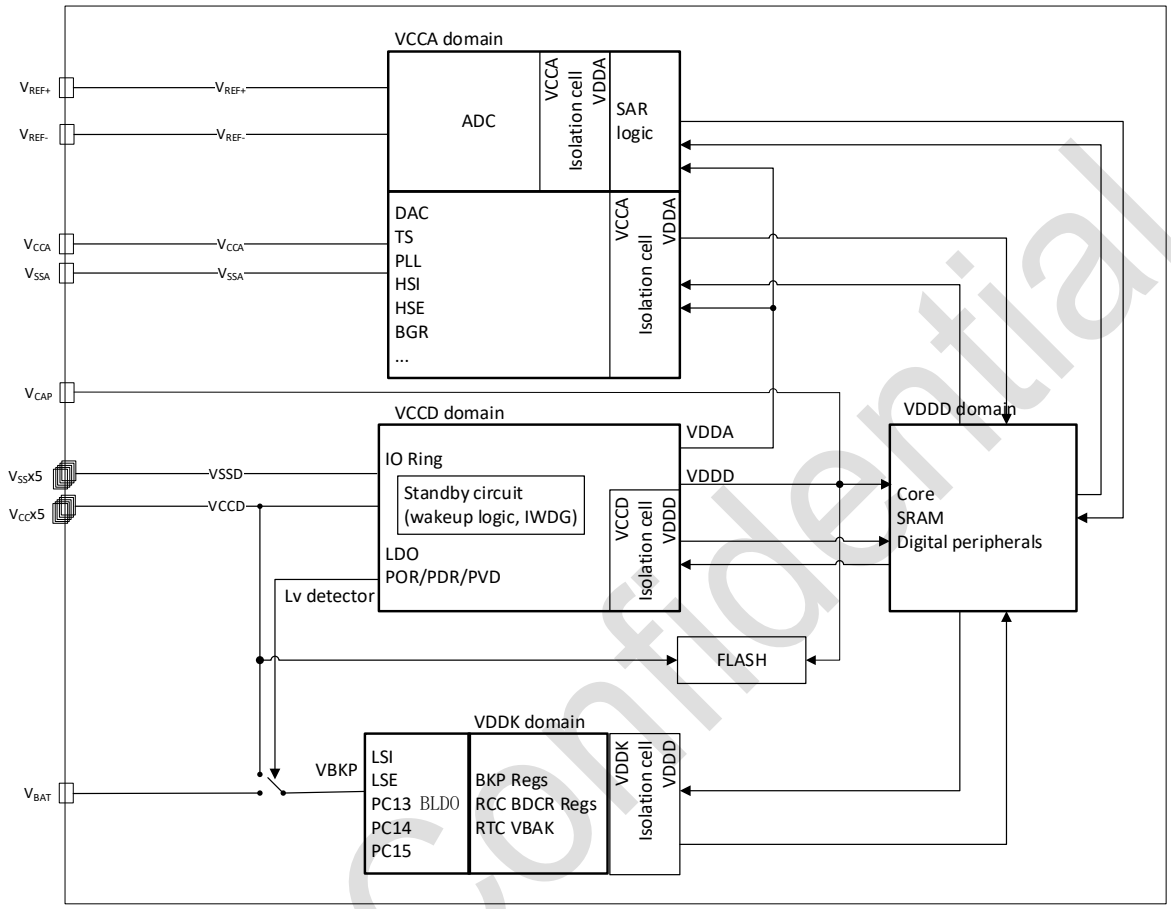


Figure 2-2 Power block diagram

Table 2-2 Power block diagram

No.	Power supply	Power value	Descriptions
1	V_{CC}	1.8 V to 3.6 V	The power is supplied to the device through the power pins.
2	V_{CAP}(1)	1.1 V	VR supplies power to the main logic circuits and SRAM inside the chip. When the MR is powered, it outputs 1.1 V. According to the soft-ware configuration, when entering the Stop mode it powered by MR or LPR, and the LPR output is determined by software.
3	V_{CCA}	1.8 V to 3.6 V	The power is supplied to the device through the power pins, with the power supply module comprising: Partial analog circuits
4	V_{BAT}	1.65 to 3.6 V	Power supplied for RTC and BKP register.

1. The stability of the main regulator is achieved by connecting an external capacitor to the V_{CAP} pin. The capacitor value C_{EXT} is determined according to the stability requirements of the system. The capacitor value C_{EXT} and ESR requirements are shown in the following table:

Table 2-3 V_{CAP} operating conditions

Symbol	Parameter	Min	Max	Unit
C_{EXT}	Capacitance of external capacitor	0.1	1	μF
ESR	ESR of external capacitor	-	0.5	Ω

2.8.2. Power monitoring

2.8.2.1. Power-on/power-down reset (POR/PDR)

The Power-on reset (POR) and Power-down reset (PDR) module is designed in the chip to provide power-on and power-down reset for the device. The module keeps working in all modes.

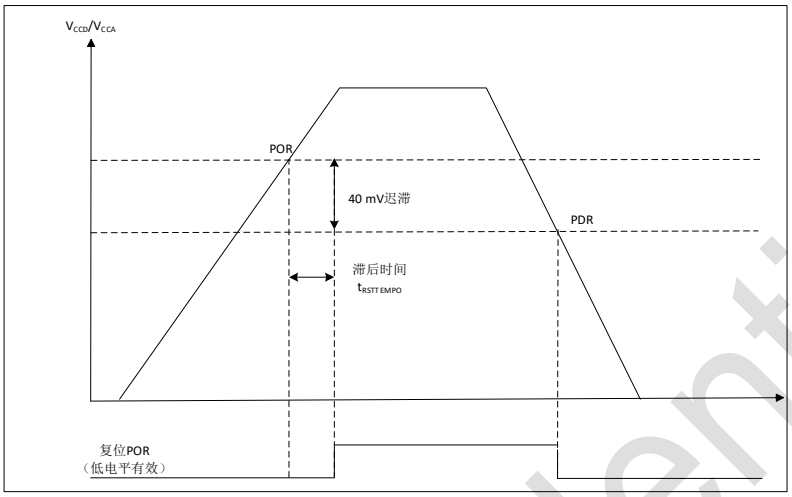


Figure 2-3 POR/PDR thresholds

2.8.2.2. Programmable voltage detector (PVD)

Programmable voltage detector (PVD) module can be used to detect the V_{CC} power supply and the detection point is configured through the register. When V_{CC} is higher or lower than the detection point of PVD, the corresponding reset flag is generated.

This event is internally connected to line 16 of EXTI, depending on the rising/falling edge configuration of EXTI line 16, when V_{CC} rises above the detection point of PVD, or V_{CC} falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

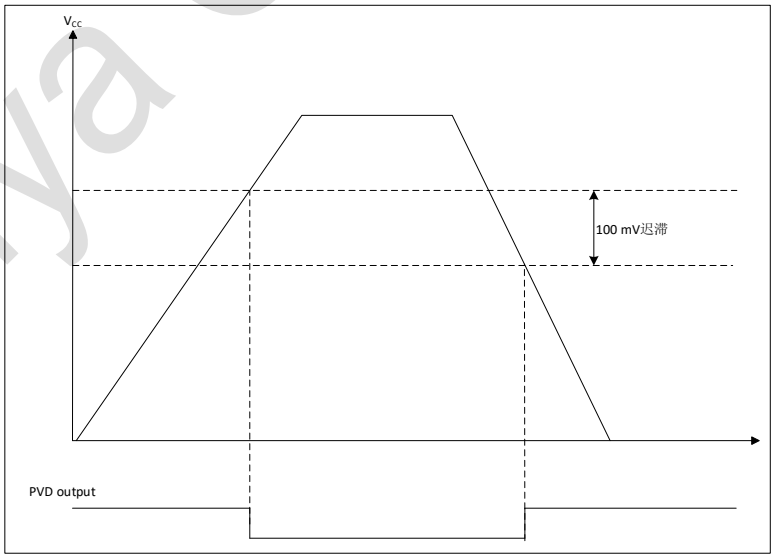


Figure 2-4 PVD threshold

2.8.3. Voltage regulator

The regulator has three operating modes:

- MR (Main regulator) is used in Run mode.
- LPR (Low power regulator) provides an option for even lower power consumption in Stop mode.
- Shutdown mode is used in CPU standby mode (LDO output is high impedance, core power is cut off, register and SRAM contents are lost).

2.8.4. Low-power mode

In addition to the Run mode, the device has three low-power modes:

- Sleep mode: Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works.
- Stop mode: In this mode, SRAM and register contents are retained. PLL, HSI and HSE are turned off and most module clocks in the V_{DDD} domain are disabled. GPIO, PVD and RTC can wake up Stop mode.
- Standby mode: The device has V_{BAT} power supply, so when the V_{CC} is powered down, the device only works in the V_{BKP} domain. Exit conditions: external reset via NRST, IWDG reset, RTC alarm wakeup, and valid edge on the WKUP pin.

2.9. Reset

Three kinds of resets are designed in the device: power reset, system reset and backup domain reset.

2.9.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Exiting Standby mode

2.9.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load (OBL) reset

2.9.3. Backup domain reset

A backup domain reset is generated when one of the following events occurs:

- Software reset, triggered by setting the BDRST bit in the RTC domain control register (RCC_BDCR).
- V_{CC} or V_{BAT} power on, if both supplies have previously been powered off.

2.10. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (floating，pull-up/down，analog) or as peripheral alternate function.The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers. OPA features are summarized as follows:

- Support read/write operations via IO Port or AHB bus
- Output states: push-pull or open drain + pull-up/down
- Output data from output data register (GPIOx_ODR) or peripheral (alternate function output)
- Speed selection for each I/O
- Input states: floating, pull-up/down, analog
- Input data to input data register (GPIOx_IDR) or peripheral (alternate function input)
- Bit set and reset register (GPIOx_BSRR) for bitwise write access to GPIOx_ODR
- Locking mechanism (GPIOx_LCKR) provided to freeze the I/O port configurations
- Analog function
- Alternate function selection registers (Max. 16 alternate functions for each IO)
- Highly flexible pin multiplexing allows the use of I/O pins as GPIOs or as one of several peripheral functions

2.11. DMA

Direct memory access (DMA) is used to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations. The device has two general-purpose dual-port DMAs (DMA1 and DMA2) with 7 and 5 channels respectively. Each channel is dedicated to managing requests for memory access from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- Single AHB Master
- Support peripherals to memory, the memory to the peripherals, memory to memory and peripherals to peripheral data transmission
- On-chip memory devices, such as Flash, an SRAM, AHB and APB peripherals, as the source and target
- All DMA channels are independently configurable:
  - Each channel is associated either with a DMA request signal from a peripheral or with a software trigger in a memory-to-memory transfer. This configuration is done by software.
  - The priority between requests is programmable by software (4 levels per channel: very high, high, medium and low) and, in equal cases, by hardware (such as a request for channel 1 taking precedence over a request for channel 2).
  - The transfer sizes of the source and target are independent (byte, half word and word), simulating packing and unpacking. The source and target addresses must be aligned by

data size.

- Programmable number of data to be transferred:0 to 65535

- Each channel generates an interrupt request. Each interrupt request is caused by one of three DMA events: transfer completion, half-transfer, or transfer error.

2.12. Interrupts and events

The PY32F403-C handles exceptions through the Cortex-M4F processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.12.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M4F processor. The NVIC can handle NMI (Non-maskable interrupts) and maskable external interrupts from outside the processor and Cortex-M4F internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 3 interrupt priority
- Support 1 NMI
- Support 57 maskable external interrupts
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.12.2. Extended interrupt/event controller (EXTI)

- EXTI adds flexibility to handle physical wire events and generates wake-up events from GPIO and dedicated modules (PVD/RTC).
- The EXTI controller has multiple channels, including up to 80 GPIOs can be connected to the 16 EXTI lines, a PVD output, and an RTC wake-up signal. GPIO and PVD can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 to 15 channel through the select signal.
- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.

- Registers in the EXTI controller latch each event. Even in Stop mode, after the processor wakes up from Stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.13. Analog-to-digital converter (ADC)

- The device has three 12-bit SARADC. The module has a total of up to 20 channels to be measured, including 16 external channels and 4 internal channels, performing conversion in single or scan mode.
- A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.
- The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.
- An efficient low-power mode is implemented to allow very low consumption at low frequency.
- Interrupt requests are triggered by the following events: end of conversion, continuous conversion and analog watchdog threshold violation (converted voltage exceeds preset limits)

2.14. Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The DAC can be configured in 8-bit or 12-bit mode, or can be used in conjunction with a DMA controller. When the DAC is operating in 12-bit mode, the data can be left justified or right justified. The DAC module has two output channels, each with a separate converter. In dual-DAC mode, the two channels can be converted independently, or they can be converted simultaneously and update the output of the two channels synchronously. The DAC can input the reference voltage V_{REF+} through the pin for more accurate conversion results. The main features are as follows:

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- Support DMA underflow error detection
- External triggers for conversion
- Input voltage reference, V_{REF+}

2.15. Timers

The different timers feature as blow:

Table 2-4 Timer characteristics

Timer type	Timers	Counter resolution	Counter type	Prescaler	DMA	Capture/compare channels	Complementary outputs
	TIM1	16-bit	Up, down, up/down	1 - 65536	Yes	4	3

Timer type	Timers	Counter resolution	Counter type	Prescaler	DMA	Capture/compare channels	Complementary outputs
Advanced-control timer	TIM8	16-bit	Up, down, up/down	1 - 65536	Yes	4	3
General-purpose timers	TIM2	16-bit	Up, down, up/down	1 - 65536	Yes	4	-
	TIM3	16-bit	Up, down, up/down	1 - 65536	Yes	4	-
	TIM4	16-bit	Up, down, up/down	1 - 65536	Yes	4	-
	TIM5	16-bit	Up, down, up/down	1 - 65536	Yes	4	-
General-purpose timers	TIM10/TIM11/TIM13/TIM14	16-bit	Up	1 - 65536	-	1	-
General-purpose timers	TIM9/TIM12	16-bit	Up	1 - 65536	-	2	-
Basic	TIM6/TIM7	16-bit	Up	1 - 65536	Yes	-	-

2.15.1. Advanced-control timer

The advanced-control timer (TIM1/TIM8) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If configured as a standard 16-bit timer, TIM1/TIM8 has the same features as the TIMx timer. If configured as the 16-bit PWM generator, TIM1/TIM8 have full modulation capability (0 to 100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the timer link feature for synchronization or event chaining.

TIM1/TIM8 supports DMA function.

2.15.2. General-purpose timers

2.15.2.1. TIM2/TIM3/TIM4/TIM5

The general-purpose timers TIM2/TIM3/TIM4/TIM5 are consist of 16-bit auto-reload counters and a 16-bit prescaler. There are four independent channels each for input capture/output compare, PWM or one-pulse mode output.

- They can work with the TIM1 by the Timer Link.
- Support DMA function
- This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

- The counter can be frozen in debug mode.

2.15.2.2. TIM10/ TIM11/ TIM13/TIM14

- The general-purpose timers TIM10/TIM11/TIM13/TIM14 are consist of 16-bit auto-reload counters and a prescaler.
- TIM10/TIM11/TIM13/TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.
- The counter can be frozen in debug mode.

2.15.2.3. TIM9/TIM12

- TIM9 and TIM12 consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM9/TIM12 features two single channels for input capture/output compare, PWM or one-pulse mode output.
- TIM9/TIM12 have complementary outputs with dead time.
- The counter can be frozen in debug mode.

2.15.3. Basic timers (TIM6/TIM7)

- The basic timer TIM6/TIM7 is consist of a 16-bit auto-reload upcounter driven by their programmable prescaler respectively.
- 16-bit auto-reload counter
- DAC synchronous circuit is triggered.
- Generate interrupt/DMA request on update event (counter overflow).

2.15.4. IWDG

Independent watchdog (IWDG) is integrated in the device, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

- The IWDG is clocked by independent RC oscillator and can work in Stop and Standby mode.
- The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application, but have lower timing accuracy constraints.
- The IWDG hardware mode can be enabled by option byte.
- IWDG is the wake-up source of Stop mode, which wakes up Stop mode by reset.
- The counter can be frozen in debug mode.

2.15.5. WWDG

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

2.15.6. SysTick timer

SysTick timer is dedicated to real-time operating systems (RTOS), but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.16. Real-time clock (RTC)

The RTC is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

- RTC is a 32-bit programmable counter with a prescaler factor of up to 2^{20} bits.
- The RTC counter clock source can be LSE, LSI and HSE/128.
- RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).
- RTC supports clock calibration.
- RTC can be frozen in debug mode.

2.17. Cyclic redundancy check calculation unit (CRC)

CRC computing unit is based on a fixed generation polynomial to obtain 32-bit CRC computing results. In other applications, CRC technology is mainly used to verify the correctness and integrity of data transmission or data storage. The CRC calculation unit contains a 32-bit data register:

- When writing to this register, it serves as an input register, allowing you to input new data for CRC calculation.
- When reading from this register, it returns the result of the previous CRC calculation.
- Each time data is written to the register, the calculation result is a combination of the previous CRC calculation result and the new one (CRC calculation is performed on the entire 32-bit word rather than byte by byte).
- You can reset the register CRC_DR to 0xFFFFFFFF by setting the RESET bit in the register CRC_CR. This operation does not affect the data in the register CRC_IDR
- Support configuration of the initial CRC value

2.18. Clock trimming controller (CTC)

The clock trimming controller (CTC) uses hardware to automatically calibrate the RC crystal oscillator internally configured at 48 MHz and serves as the clock source of the USBD module. The CTC module calibrates the clock frequency of HSI based on an external high-precision reference signal source, and automatically or manually adjusts the calibration value to obtain an accurate PLL48M clock.

The CTC module provides the following functions:

- Three external reference sources: GPIO, LSE clock and USBD_SOF.
- Provide software reference synchronization pulse.
- Hardware calibration automatically, no software operation.
- 16 bits calibration counter with reference source capture and overload capabilities.
- 8 bits clock calibration base value for frequency evaluation and automatic calibration.
- Flag bits and interrupts that indicate the state of clock calibration: calibration OK flag (CKOKIF),

warning flag (CKWARNIF), and error flag (ERRIF).

2.19. System configuration controller (SYSCFG)

The SYSCFG module provides the following functions:

- All IO noise filter controls enabled.
- EXTI IO select control.
- Mapping the initial program area according to different boot modes
- DMA peripheral channel selection control
- TIMERs breakin and ETR control

2.20. Debug Support (DBG)

The MCU DBG module assists the debugger with the following functions:

- Support Sleep, Stop and Standby mode
- When the CPU enters the HALT mode, the control timer or watchdog stops counting or continues counting
- Block I^2C1 and I^2C2 SMBUS timeouts when the CPU is in HALT mode
- Block CANFD receive register updates when the CPU is in HALT mode
- Assigns tracking pins

The MCUDBG register also provides chip ID encoding. This ID encoding can be accessed by a JTAG or SW debug interface, or by a user program.

2.21. Secure digital input/output interface (SDIO)

The SD/SDIO MMC card host interface provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards, SDIO cards and the CE-ATA device.

The SDIO features include the following:

- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0
- Full compliance with MultiMediaCard System Specification Version 4.2
- Fully compliance with the CE-ATA digital protocol Rev1.1
- Supports command completion signals and interrupts to the hostprocessor
- Command completion signal disabed

The SDIO does not have an SPI-compatible communication mode and it is supported by either SD I/O-only cards or the I/O portion of combo cards. Some of these commands have no use in SD I/O devices, such as erase commands, and thus are not supported in the SDIO. In addition, several commands are different between SD memory cards and SD I/O cards and thus are not supported in the SDIO. MMC4.1 does not support boot from DDR.

2.22. Inter-integrated circuit interface (I^2C)

The I^2C (Inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I^2C bus. It provides multimaster capability, and controls all I^2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm) and Fast-mode (Fm) .

I^2C features:

- Multimaster capability: can be master or slave
- Support different communication speeds
  - Standard mode (Sm): up to 100 kHz
  - Fast mode (Fm): up to 400 kHz
- As master
  - Generate clock
  - Generation of Start and Stop
- As slave
  - Programmable I^2C address detection
  - Dual-address capability that responds to two secondary addresses
  - Discovery of the Stop bit
- 7-bit/10-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I^2C busy flag bit
- Error flag
  - Master arbitration loss
  - ACK failure after address/data transfer
  - Start/Stop error
  - Overrun/Underrun (clock stretching function disable)
- Optional clock stretching
- Single-byte buffer with DMA capability
- Software reset
- Analog noise filter function
- Support SMBus

2.23. Universal synchronous/asynchronous receiver transmitter (USART)

The PY32F403-C contains 5 universal synchronous/asynchronous receiver transmitter (USART) and supports ISO7816, LIN and IrDA.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baud rate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USART features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baud rate shared by transmit and receive, up to 4.5 Mbit/s
- Automatic baud rate detection
- Programmable data length of 8 or 9 bits
- Configurable Stop bits (0.5, 1, 1.5 or 2 bits)
- The transmitter provides a clock for synchronous transmission
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control
- Receive/transmit bytes by DMA buffer
- Transfer detection flag
  - Receive buffer full
  - Send empty buffer
  - End of transmission flags
- Parity control
  - Transmit parity bit
  - Check the received data byte
- Flagged interrupt sources
  - CTS change
  - Transmit data register empty
  - Transmission complete
  - Receive full data register

- Bus idle detected
- Overflow error
- Frame error
- Noise operation
- Error detection
- LIN break detection

- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection Two receiver wake-up modes: Address bit (MSB, 9th bit), Idle line

2.24. Serial peripheral interface (SPI)

PY32F403-C contains three SPIs. The serial peripheral interface (SPI) protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices. This interface can be configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- 8 Master mode baud rate prescaling factors (Max $f_{PCLK}/4$)
- Slave mode frequency (Max $f_{PCLK}/4$)
- Both Master and Slave modes can be managed by software or hardware NSS: dynamic change of Master/Slave operating mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Motorola mode
- Interrupt-causing Master mode faults or overloads
- Two 64 (16x4)-bit transmission and reception buffer with DMA capability: R_X and T_X FIFOs

2.25. I²S features:

- 3 x I²S bus interfaces with sampling rate 8 to 192 kHz
- Support master and slave mode, full duplex and simplex communications

The I²S bus provides a standard communication interface for digital audio applications over a 3-wire serial line. Three I²S bus interfaces operate at 16/32 bit resolution in master or slave mode, with pins

multiplexed with SPI1, SPI2 and SPI3. Support audio sampling frequencies of 8 to 192 kHz, and the accuracy error is less than 0.5%. A DMA controller is available for all I^2S interfaces.

2.26. External serial memory controller (ESMC)

ESMC (External serial memory controller) is a dedicated communication interface for single, dual, quad and dual-quad channel SPI interface memory (NOR Flash, PSRAM, etc.). It can run in either of the following two modes:

- Indirect mode: all operations are performed using the QUADSPI register
- Memory mapped mode: external Flash memory is mapped to the device address space, and is regarded as internal memory in the system.

Using the dual memory mode, that is, accessing two Quad SPI memories at the same time, you can achieve twice the throughput and storage capacity similar to Octal SPI memory.

- Two functional modes: indirect and memory mapped
- Can transmit/receive 8 bits simultaneously
- Dual flash mode, which allows simultaneous transmission/reception of 8 bits by accessing two flashes in parallel
- Support SDR and DDR
- Fully programmable opcodes for indirect and memory-mapped modes
- Fully programmable frame formats for indirect and memory-mapped modes
- Integrated FIFO for reception and transmission
- Allow only 32-bit data access
- DMA channel for indirect mode operation
- Interrupt generation on FIFO operation completion

2.27. USB 2.0 full-speed module

PY32F403-C contains 1 USB 2.0 full speed module. USB peripheral implements the interface between USB2.0 full speed bus and APB1 bus. It supports USB suspend/restore operation and can stop the device clock to achieve low power consumption. The main features are as follows:

- Comply with the technical specifications of USB 2.0 full speed devices
- Configurable with 1 to 8 USB endpoints
- CRC (cyclic redundancy check) generation/check, reverse non-return to zero inverted (NRZI) encoding/decoding and bit filling
- Support synchronous transmission
- Support a dual buffer mechanism for batch/synchronous endpoints
- USB suspend and restore operations are supported
- Frame lock clock pulse generation

2.28. CANFD

The PY32F403-C contains 1 CANFD communication interface module.

The controller area network (CAN) bus is a bus standard that can realize the communication between microprocessors or devices without a host. The CAN FD controller follows the CAN bus CAN2.0 (2.0 A, CAN2.0 B) and CAN FD protocols.

The CAN bus controller can handle data sending and receiving on the bus. In this product, the CANFD controller has 12 groups of filters. Filters are used to select messages for the application to receive.

The application program in the CAN FD controller can transmit 1 primary transmit buffer (PTB) and 3 secondary transmit buffers (STB) which help to send the sending data to the bus, and the sending scheduler determines the sending order of the mailboxes. The bus data is obtained through three receive buffers (RB). The 3 STBs and 3 RBs can be understood as a 3-stage FIFO and a 3-stage FIFO, and the FIFO is completely controlled by hardware.

The CANFD bus controller also supports Time-trigger communication.

- Full support for CAN2.0A/CAN2.0B/CANFD protocols
- CAN 2.0 supports a maximum communication baud rate of 1 Mbit/s
- The baud rate ranges from 1 to 1/32. The baud rate is flexibly configured
- Three receive buffers
  - FIFO mode
  - Error or non-received data does not overwrite stored messages
- One high-priority primary send buffer PTB
- Three sub-send buffers STB
  - FIFO mode
  - Priority arbitration mode
- 12 separate sets of filters
  - Supports 11-bit standard ID and 29-bit extended ID
  - Programmable ID CODE bit and MASK bit
- Both PTB/STB support single transmit mode
- Support silent mode
- Support loopback mode
- Support capturing transmission error types and locating quorum failure locations
- Programmable error warning value
- Support ISO11898-4 time trigger CANFD and receive time stamp

2.29. SWD

An ARM SWD interface allows serial debugging tools to be connected to the PY32F403-C.

3. Pinouts and pin descriptions

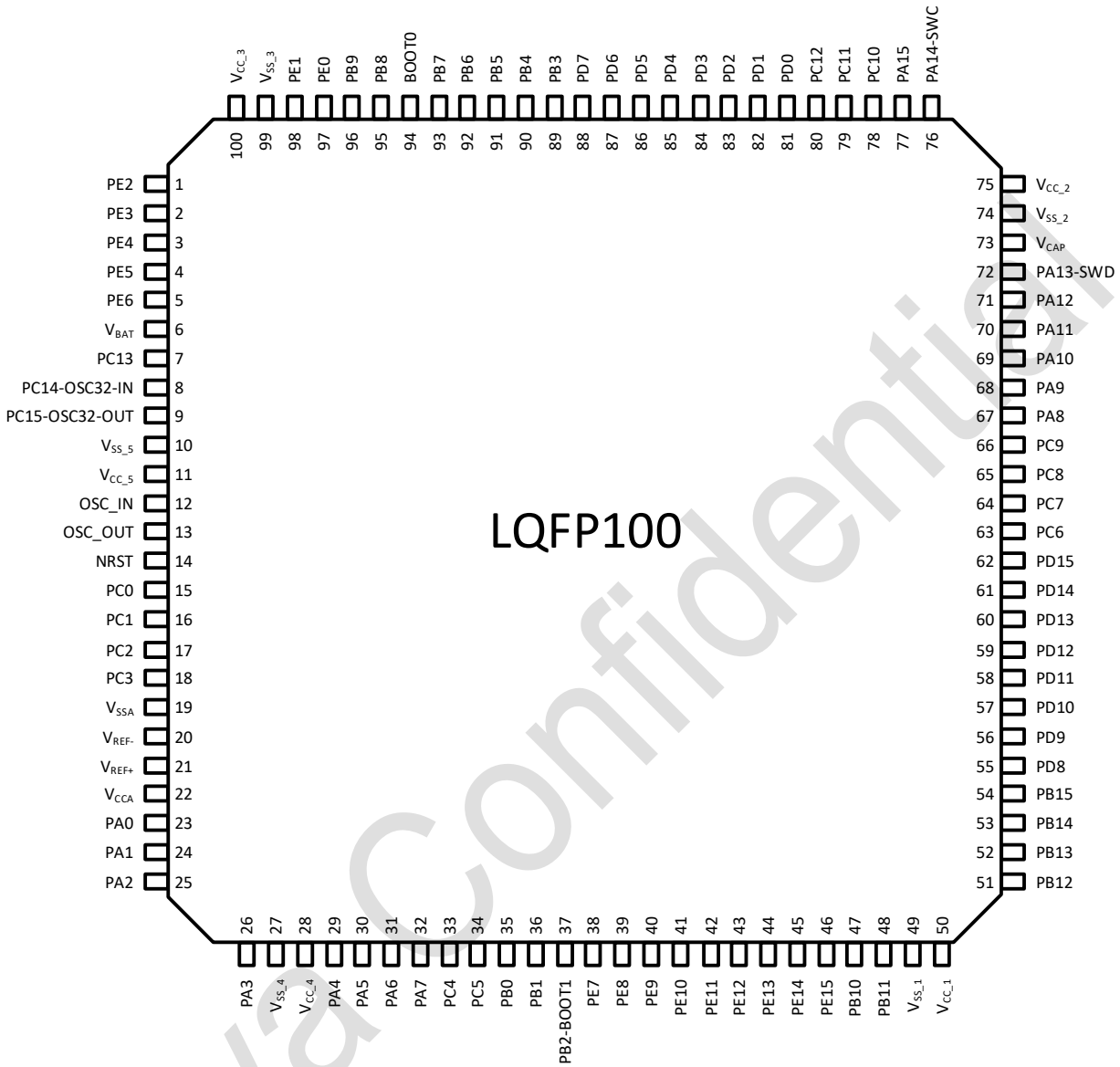


Figure 3-1 LQFP100 Pinout1 PY32F403V1xT7 (Top view)

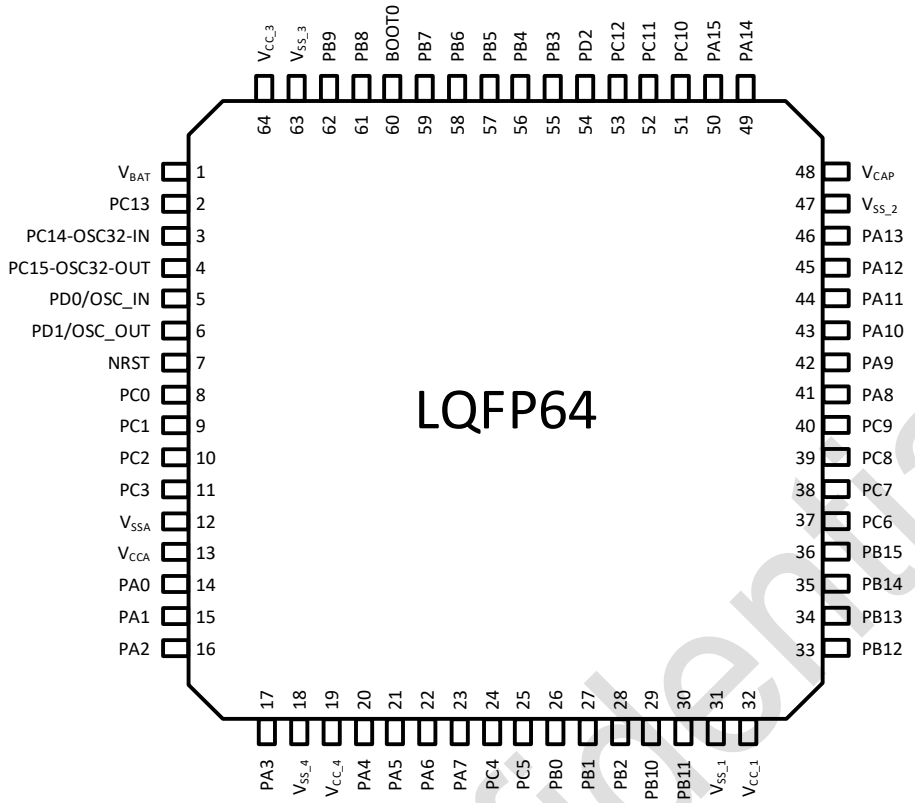


Figure 3-2 LQFP64 Pinout1 PY32F403R1xT7 (Top view)

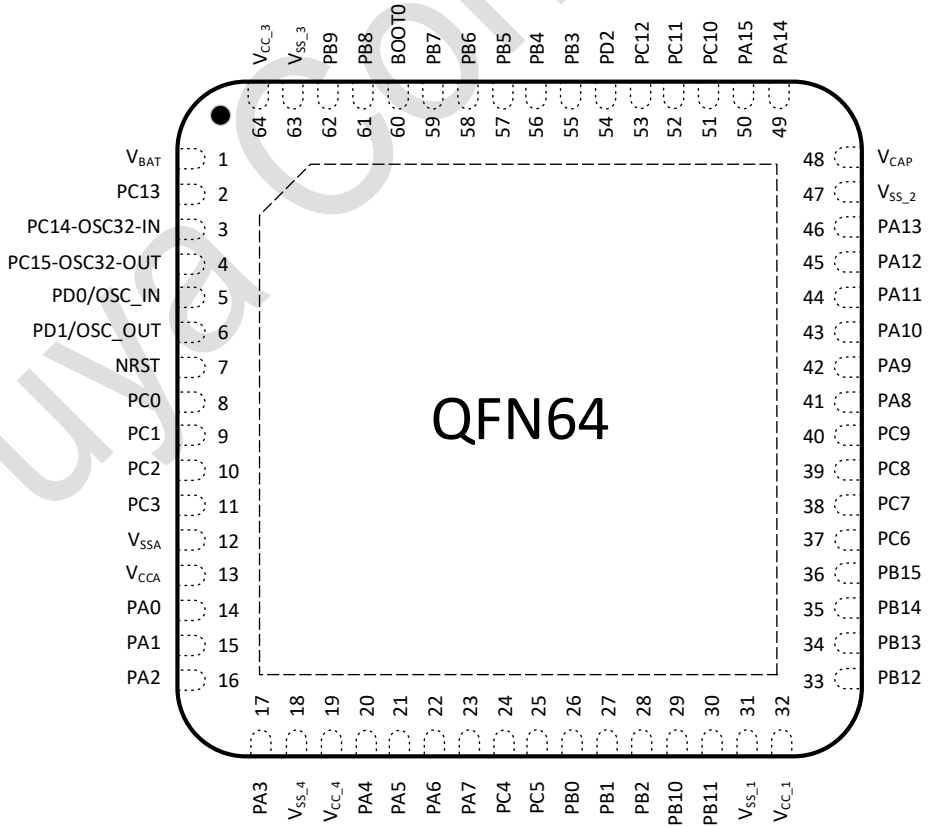


Figure 3-3 QFN64 Pinout1 PY32F403R1xU7 (Top view)

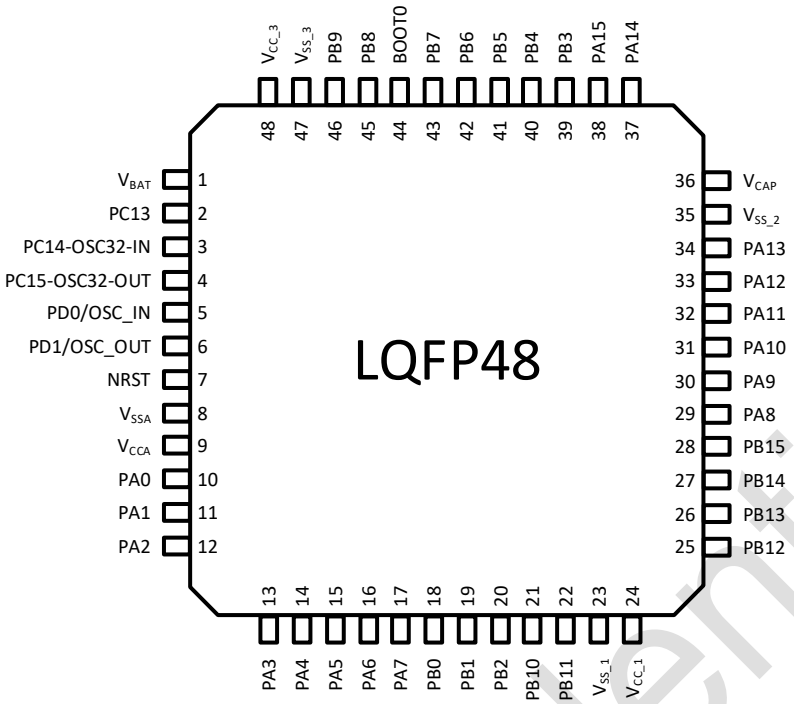


Figure 3-4 LQFP48 Pinout1 PY32F403C1xT7 (Top view)

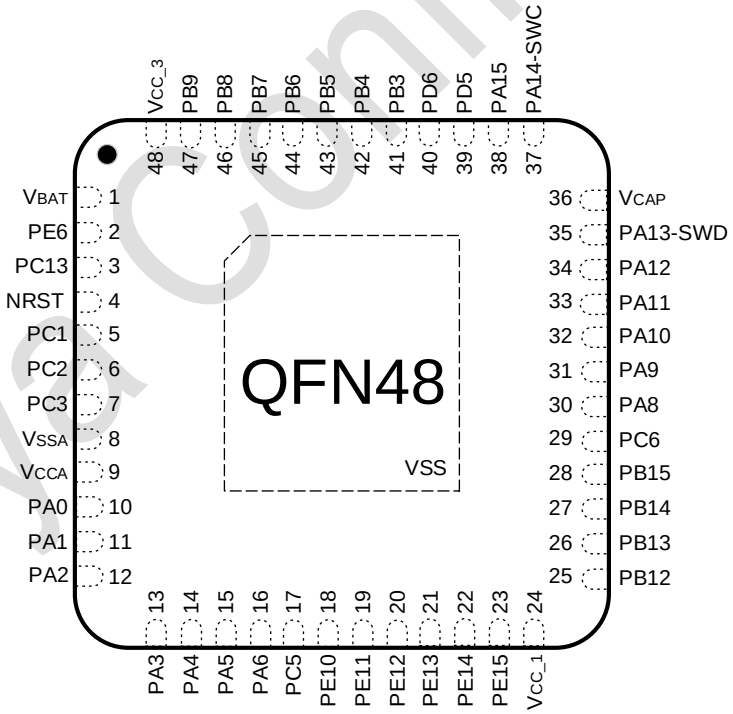


Figure 3-5 QFN48 Pinout1 PY32F403C1xU7 (Top view)

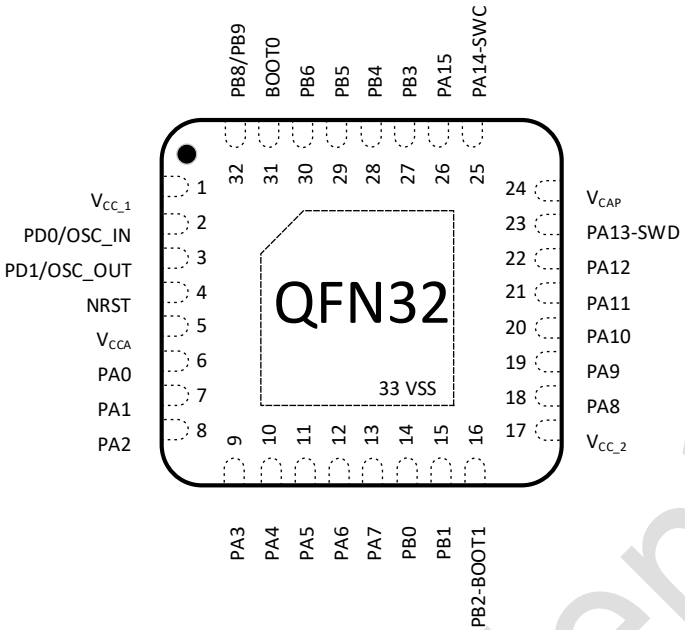


Figure 3-6 QFN32 Pinout1 PY32F403K1xU7 (Top view)

Table 3-1 Legend/abbreviations used in the pinout table

Timer type		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		I	Input-only pin
		I/O	Input / output pin
		NC	No internal connection
I/O structure		FT	5 V tolerant I/O
		FT_u	5 V tolerant with USB function
		TT	3.3 V tolerant I/O
		TT_a	3.3 V tolerant with analog switch
		NRST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		-	Unless otherwise specified, all ports are used as floating inputs between and after reset
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected/enabled through peripheral registers

Table 3-2 Pin definitions

Packages					Pin name	Pin type	I/O structure	Reset(1)	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
1	-	-	-	-	PE2	I/O	FT	PE2	EVENT_OUT	-
2	-	-	-	-	PE3	I/O	FT	PE3	EVENT_OUT	-
3	-	-	-	-	PE4	I/O	FT	PE4	EVENT_OUT	-
4	-	-	-	-	PE5	I/O	FT	PE5	TIM9_CH1 EVENT_OUT	-
5	-	-	2	-	PE6	I/O	FT	PE6	TIM9_CH2 ENENT_OUT	WKUP3
6	1	1	1	-	V_{BAT}	S	-	V_{BAT}	-	-
7	2	2	3	-	PC13-TAMPER RTC (2)(3)(5)	I/O	TT	PC13	EVENT_OUT	TAMPER-RTC WKUP2
8	3	3	-	-	PC14-OSC32_IN(2)(3)	I/O	TT	PC14	EVENT_OUT	OSC32_IN
9	4	4	-	-	PC15- OSC32_OUT(2)(3)	I/O	TT	PC15	EVENT_OUT	OSC32_OUT
10	-	-	-	-	V_{SS_5}	G	-	V_{SS_5}	-	-
11	-	-	-	-	V_{CC_5}	S	-	V_{CC_5}	-	-
12	5	5	-	2	OSC_IN(6)	I	-	OSC_IN	-	-
13	6	6	-	3	OSC_OUT(6)	O	-	OSC_OUT	-	-
14	7	7	4	4	NRST	-	-	NRST	-	-
15	8	-	-	-	PC0	I/O	TT_a	PC0	EVENT_OUT	ADC123_IN10
16	9	-	5	-	PC1	I/O	TT_a	PC1	ESMC_IO4 EVENT_OUT	ADC123_IN11
17	10	-	6	-	PC2	I/O	TT_a	PC2	ESMC_IO5	ADC123_IN12

Packages					Pin name	Pin type	I/O structure	Reset(1)	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
									EVENT_OUT	
18	11	-	7	-	PC3	I/O	TT_a	PC3	ESMC_IO6 EVENT_OUT	ADC123_IN13
19	12	8	8	-	V_{SSA}	G	-	V_{SSA}	-	-
20	-	-	-	-	V_{REF-}	S	-	V_{REF-}	-	-
21	-	-	-	-	V_{REF+}	S	-	V_{REF+}	-	-
22	13	9	9	5	V_{CCA}	S	-	V_{CCA}	-	-
23	14	10	10	6	PA0-WKUP1	I/O	TT_a	PA0	WKUP1 USART2_CTS TIM8_ETR TIM2_CH1_ETR TIM5_CH1 EVENT_OUT	ADC123_IN0 WKUP1
24	15	11	11	7	PA1	I/O	TT_a	PA1	USART2_RTS TIM2_CH2 TIM5_CH2 EVENT_OUT	ADC123_IN1
25	16	12	12	8	PA2	I/O	TT_a	PA2	USART2_TX TIM2_CH3 TIM5_CH3 TIM9_CH1 ESMC_SS0	ADC123_IN2 WKUP4

Packages					Pin name	Pin type	I/O structure	Reset(1)	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
									EVENT_OUT	
26	17	13	13	9	PA3	I/O	TT_a	PA3	USART2_RX	ADC123_IN3
									TIM2_CH4	
									TIM5_CH4	
									TIM9_CH2	
									ESMC_CLK	
									EVENT_OUT	
27	18	-	-	-	V_{SS_4}	G	-	V_{SS_4}	-	-
28	19	-	-	-	V_{CC_4}	S	-	V_{CC_4}	-	-
29	20	14	14	10	PA4	I/O	TT_a	PA4	USART2_CK	ADC123_IN4 DAC_OUT1
									SPI1_NSS	
									EVENT_OUT	
30	21	15	15	11	PA5	I/O	TT_a	PA5	SPI1_SCK	ADC123_IN5 DAC_OUT2
									EVENT_OUT	
31	22	16	16	12	PA6	I/O	TT_a	PA6	SPI1_MISO	ADC123_IN6
									TIM8_BKIN	
									TIM3_CH1	
									TIM13_CH1	
									ESMC_IO3	
									EVENT_OUT	
32	23	17	-	13	PA7	I/O	TT_a	PA7	SPI1_MOSI	ADC123_IN7
									TIM8_CH1N	

Packages					Pin name	Pin type	I/O structure	Reset(1)	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
									TIM3_CH2	
									TIM14_CH1	
									ESMC_IO2	
									EVENT_OUT	
33	24	-	-	-	PC4	I/O	TT_a	PC4	ESMC_IO7	ADC123_IN14
									EVENT_OUT	
34	25	-	17	-	PC5	I/O	TT_a	PC5	EVENT_OUT	ADC123_IN15 WKUP5
									I^2S1_MCK	
35	26	18	-	14	PB0	I/O	TT_a	PB0	TIM1_CH2N	ADC123_IN8
									TIM8_CH2N	
									TIM3_CH3	
									ESMC_IO1	
									SPI3_SCK	
									EVENT_OUT	
36	27	19	-	15	PB1	I/O	TT_a	PB1	TIM1_CH3N	ADC123_IN9
									TIM8_CH3N	
									TIM3_CH2	
									ESMC_IO0	
									EVENT_OUT	
37	28	20	-	16	PB2-BOOT1	I/O	FT	PB2/BOOT1	BOOT1	-
									EVENT_OUT	
38	-	-	-	-	PE7	I/O	FT	PE7	TIM1_ETR	-

Packages					Pin name	Pin type	I/O structure	Reset[1]	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
39	-	-	-	-	PE8	I/O	FT	PE8	TIM1_CH1N	-
40	-	-	-	-	PE9	I/O	FT	PE9	TIM1_CH1	-
41	-	-	18	-	PE10	I/O	FT	PE10	TIM1_CH2N	-
									ESMC_CLK	
									EVENT_OUT	
42	-	-	19	-	PE11	I/O	FT	PE11	TIM1_CH2	-
									ESMC_SS3	
									EVENT_OUT	
43	-	-	20	-	PE12	I/O	FT	PE12	TIM1_CH3N	-
									ESMC_IO0	
									EVENT_OUT	
44	-	-	21	-	PE13	I/O	FT	PE13	TIM1_CH3	-
									ESMC_IO1	
									EVENT_OUT	
45	-	-	22	-	PE14	I/O	FT	PE14	TIM1_CH4	-
									ESMC_IO2	
									EVENT_OUT	
46	-	-	23	-	PE15	I/O	FT	PE15	TIM1_BKIN	-
									ESMC_IO3	
									EVENT_OUT	
47	29	21	-	-	PB10	I/O	FT	PB10	I^2C2_SCL	-
									USART3_TX	

Packages					Pin name	Pin type	I/O structure	Reset(1)	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
									TIM2_CH3	
									ESMC_CLK	
									EVENT_OUT	
48	30	22	-	-	PB11	I/O	FT	PB11	I^2C2_SDA	-
									USART3_RX	
									TIM2_CH4	
									ESMC_SS1	
									EVENT_OUT	
49	31	23	-	-	V_{SS_1}	G	-	V_{SS_1}	-	-
50	32	24	24	1	V_{CC_1}	S	-	V_{CC_1}	-	-
51	33	25	25	-	PB12	I/O	FT	PB12	I^2C2_SMBA	-
									USART3_CK	
									SPI2_NSS	
									TIM1_BKIN	
									SPI2_NSS	
									EVENT_OUT	
52	34	26	26	-	PB13	I/O	FT	PB13	USART3_CTS	-
									SPI2_SCK	
									TIM1_CH1N	
									SPI2_MOSI	
									EVENT_OUT	
53	35	27	27	-	PB14	I/O	FT	PB14	USART3_RTS	-

Packages					Pin name	Pin type	I/O structure	Reset(1)	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
									SPI2_MISO	
									TIM1_CH2N	
									TIM12_CH1	
									EVENT_OUT	
54	36	28	28	-	PB15	I/O	FT	PB15	SPI2_MOSI	-
									TIM1_CH3N	
									TIM12_CH2	
									SPI2_MOSI	
									EVENT_OUT	
55	-	-	-	-	PD8	I/O	FT	PD8	USART3_TX	-
									EVENT_OUT	
56	-	-	-	-	PD9	I/O	FT	PD9	USART3_RX	-
									EVENT_OUT	
57	-	-	-	-	PD10	I/O	FT	PD10	USART3_CK	-
									EVENT_OUT	
58	-	-	-	-	PD11	I/O	FT	PD11	USART3_CTS	-
									EVENT_OUT	
59	-	-	-	-	PD12	I/O	FT	PD12	TIM4_CH1	-
									USART3_RTS	
									EVENT_OUT	
60	-	-		-	PD13	I/O	FT	PD13	TIM4_CH2	-
									EVENT_OUT	

Packages					Pin name	Pin type	I/O structure	Reset[1]	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
61	-	-	-	-	PD14	I/O	FT	PD14	TIM4_CH3	-
									EVENT_OUT	
62	-	-	-	-	PD15	I/O	FT	PD15	TIM4_CH4	-
									EVENT_OUT	
63	37	-	29	-	PC6	I/O	FT	PC6	USART4_CK	-
									TIM8_CH1	
									TIM3_CH1	
									SDIO_D6	
									I^2S2_MCK	
									EVENT_OUT	
64	38	-	-	-	PC7	I/O	FT	PC7	USART4_CTS	-
									TIM8_CH2	
									TIM3_CH2	
									SDIO_D7	
									I^2S3_MCK	
									EVENT_OUT	
65	39	-	-	-	PC8	I/O	FT	PC8	USART4_RTS	-
									TIM8_CH3	
									TIM3_CH3	
									SDIO_D0	
									EVENT_OUT	
66	40	-	-	-	PC9	I/O	FT	PC9	TIM8_CH4	-

Packages					Pin name	Pin type	I/O structure	Reset[1]	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
									TIM3_CH4	
									SDIO_D1	
									EVENT_OUT	
67	41	29	30	18	PA8	I/O	FT	PA8	MCO	-
									USART1_CK	
									TIM1_CH1	
									EVENT_OUT	
68	42	30	31	19	PA9	I/O	FT	PA9	USART1_TX	-
									TIM1_CH2	
									EVENT_OUT	
69	43	31	32	20	PA10	I/O	FT	PA10	USART1_RX	-
									CTC_SYNC	
									TIM1_CH3	
									EVENT_OUT	
70	44	32	33	21	PA11	I/O	FT_u	PA11	USART1_CTS	USB_DM
									TIM1_CH4	
									CAN_RX	
									EVENT_OUT	
71	45	33	34	22	PA12	I/O	FT_u	PA12	USART1_RTS	USB_DP
									TIM1_ETR	
									CAN_TX	
									EVENT_OUT	

Packages					Pin name	Pin type	I/O structure	Reset[1]	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
72	46	34	35	23	PA13	I/O	FT	JTMS-SWDIO	JTMS-SWDIO	-
									EVENT_OUT	
73	48	36	36	24	V_{CAP}[4]	-	-	V_{CAP}	-	-
74	47	35	-	-	V_{SS_2}	G	-	V_{SS_2}	-	-
75	-	-	-	17	V_{CC_2}	S	-	V_{CC_2}	-	-
76	49	37	37	25	PA14	I/O	FT	JTCK-SWCLK	JTCK-SWCLK	-
									EVENT_OUT	
77	50	38	38	26	PA15	I/O	FT	JTDI	JTDI	-
									SPI3_NSS	
									SPI1_NSS	
									TIM2_CH1_ETR	
									SPI3_NSS	
									EVENT_OUT	
78	51	-	-	-	PC10	I/O	FT	PC10	USART4_TX	-
									USART3_TX	
									SDIO_D2	
									SPI_SCK	
									EVENT_OUT	
79	52	-	-	-	PC11	I/O	FT	PC11	USART4_RX	-
									USART3_RX	
									SDIO_D3	
									SPI_NSS	

Packages					Pin name	Pin type	I/O structure	Reset[1]	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
									EVENT_OUT	
80	53	-	-	-	PC12	I/O	FT	PC12	USART5_TX	-
									USART3_CK	
									SDIO_CK	
									SPI_MOSI	
									EVENT_OUT	
81	5	5	-	2	PD0[6]	I/O	FT	-	CAN_RX	-
									EVENT_OUT	
82	6	6	-	3	PD1[6]	I/O	FT	-	CAN_TX	-
									EVENT_OUT	
83	54	-	-	-	PD2	I/O	FT	PD2	TIM3_ETR	-
									USART5_RX	
									SDIO_CMD	
									EVENT_OUT	
84	-	-	-	-	PD3	I/O	FT	PD3	USART2_CTS	-
									USART5_CK	
									ESMC_SS2	
									EVENT_OUT	
85	-	-	-	-	PD4	I/O	FT	PD4	USART2_RTS	-
									USART5_CTS	
									ESMC_IO4	
									EVENT_OUT	

Packages					Pin name	Pin type	I/O structure	Reset[1]	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
86	-	-	39	-	PD5	I/O	FT	PD5	USART2_TX USART5_RTS ESMC_IO5 EVENT_OUT	-
87	-	-	40	-	PD6	I/O	FT	PD6	USART2_RX ESMC_IO6 EVENT_OUT	-
88	-	-	-	-	PD7	I/O	FT	PD7	USART2_CK ESMC_IO7 EVENT_OUT	-
89	55	39	41	27	PB3	I/O	FT	JTDO	JTDO SPI3_SCK SPI1_SCK TIM2_CH2 EVENT_OUT	-
90	56	40	42	28	PB4	I/O	FT	NJTRST	NJTRST SPI3_MISO SPI1_MISO TIM3_CH1 EVENT_OUT	-
91	57	41	43	29	PB5	I/O	TT	PB5	I^2C1_SMBA SPI3_MOSI	-

Packages					Pin name	Pin type	I/O structure	Reset[1]	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
									SPI1_MOSI	
									TIM3_CH2	
									SPI3_MOSI	
									EVENT_OUT	
92	58	42	44	30	PB6	I/O	FT	PB6	I^2C1_SCL	-
									USART1_TX	
									TIM4_CH1	
									EVENT_OUT	
93	59	43	45	-	PB7	I/O	FT	PB7	I^2C1_SDA	-
									USART1_RX	
									TIM4_CH2	
									EVENT_OUT	
94	60	44	-	31	BOOT0	I	-	BOOT0	-	-
95	61	45	46	32	PB8[6]	I/O	FT	PB8	I^2C1_SCL	-
									TIM4_CH3	
									TIM10_CH1	
									CAN_RX	
									SDIO_D4	
									EVENT_OUT	
96	62	46	47	32	PB9[6]	I/O	FT	PB9	I^2C1_SDA	-
									TIM4_CH4	
									TIM11_CH1	

Packages					Pin name	Pin type	I/O structure	Reset(1)	Pin functions	
LQFP100 V1	LQFP 64 R1 QFN64 R1	LQFP48 C1	QFN48 C1	QFN32 K1					Alternate functions	Additional functions
									CAN_TX	
									SDIO_D45	
									EVENT_OUT	
97	-	-	-	-	PE0	I/O	FT	PE0	TIM4_ETR	-
									EVENT_OUT	
98	-	-	-	-	PE1	I/O	FT	PE1	EVENT_OUT	-
99	63	47	-	-	V_{SS_3}	G	-	V_{SS_3}	-	-
100	64	48	48	-	V_{CC_3}	S	-	V_{CC_3}	-	-

1. Available functions depend on the specified device. If multiple peripherals share the same I/O pin, to avoid conflicts between these functions, only one peripheral can be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
2. The PC13, PC14, and PC15 are supplied through a power switch. The switch is current-limited (3 mA sourcing), thus GPIO PC13 to PC15 output mode have restrictions:
   1) Maximum rate 2 MHz, load ≤30 pF.
   2) Cannot be used as current sources (e.g., LED driving).
3. The main functions after the first backup domain is powered on. After this it depends on the contents of the backup registers, even after a reset (as these registers are not controlled by the main area reset).
4. LDO core-powered output (intern al circuits only, external 0.1 to 1 μF decoupling capacitor required).
5. When only V_{BAT} is powered, PC13 may be in one of the following states: analog mode, input mode, push-pull with pull-up, or push-pull with pull-down. Design recommendations:
   1) Add a 1 to 10 MΩ resistor to ground on PC13 to prevent leakage current when the pin is in input mode.
   2) Resistor selection (as in recommendation 1) should account for the output current when PC13 is configured as push-pull with pull-up.
6. Two IO ports are lead out on the same pin, only one of the IO ports can be used at the same time, and the other IO must be configured in analog mode (MODEy [1: 0] is 0B11).

3.1. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-3 Port A alternate functions mapping

PortA	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	-	USART2_CTS	-	-	TIM8_ETR	TIM2_CH1_ETR	TIM5_CH1	-	-	-	-	-	-	-	EVENT_OUT
PA1	-	-	USART2_RTS	-	-	-	TIM2_CH2	TIM5_CH2	-	-	-	-	-	-	-	EVENT_OUT
PA2	-	-	USART2_TX	-	-	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	ESMC_SS0	-	-	-	-	EVENT_OUT
PA3	-	-	USART2_RX	-	-	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	ESMC_CLK	-	-	-	-	EVENT_OUT
PA4	-	-	USART2_CK	SPI1_NSS	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PA5	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PA6	-	-	-	SPI1_MISO	-	TIM8_BKIN	TIM3_CH1	-	TIM13_CH1	-	ESMC_IO3	-	-	-	-	EVENT_OUT
PA7	-	-	-	SPI1_MOSI	-	TIM8_CH1N	TIM3_CH2	-	TIM14_CH1	-	ESMC_IO2	-	-	-	-	EVENT_OUT
PA8	MCO	-	USART1_CK	-	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PA9	-	-	USART1_TX	-	TIM1_CH2	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PA10	-	-	USART1_RX	CTC_SYNC	TIM1_CH3	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PA11	-	-	USART1_CTS	-	TIM1_CH4	-	-	-	-	-	CAN_RX	-	-	-	-	EVENT_OUT
PA12	-	-	USART1_RTS	-	TIM1_ETR	-	-	-	-	-	CAN_TX	-	-	-	-	EVENT_OUT
PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PA15	JTDI	-	SPI3_NSS	SPI1_NSS	-	-	TIM2_CH1_ETR	-	-	-	-	-	-	-	SPI3_NSS	EVENT_OUT

3.2. Alternate functions selected through GPIOB_AFR registers for port B

Table 3-4 Port B alternate function mapping

PortB	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	-	-	-	-	TIM1_CH2N	TIM8_CH2N	TIM3_CH3	-	-	-	ESMC_IO1	-	-	-	SPI3_SCK	EVENT_OUT
PB1	-	-	-	-	TIM1_CH3N	TIM8_CH3N	TIM3_CH4	-	-	-	ESMC_IO0	-	-	-	-	EVENT_OUT
PB2	BOOT1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PB3	JTDO	-	SPI3_SCK	SPI1_SCK	-	-	TIM2_CH2	-	-	-	-	-	-	-	-	EVENT_OUT
PB4	NJTRST	-	SPI3_MISO	SPI1_MISO	-	-	TIM3_CH1	-	-	-	-	-	-	-	-	EVENT_OUT
PB5	-	I2C1_SMBA	SPI3_MOSI	SPI1_MOSI	-	-	TIM3_CH2	-	-	-	-	-	-	-	SPI3_MOSI	EVENT_OUT
PB6	-	I2C1_SCL	USART1_TX	-	-	-	TIM4_CH1	-	-	-	-	-	-	-	-	EVENT_OUT
PB7	-	I2C1_SDA	USART1_RX	-	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	EVENT_OUT
PB8	-	I2C1_SCL	-	-	-	-	TIM4_CH3	-	TIM10_CH1	-	CAN_RX	SDIO_D4	-	-	-	EVENT_OUT
PB9	-	I2C1_SDA	-	-	-	-	TIM4_CH4	-	TIM11_CH1	-	CAN_TX	SDIO_D5	-	-	-	EVENT_OUT
PB10	-	I2C2_SCL	USART3_TX	-	-	-	TIM2_CH3	-	–	-	ESMC_CLK	-	-	-	-	EVENT_OUT
PB11	-	I2C2_SDA	USART3_RX	-	-	-	TIM2_CH4	-	–	-	ESMC_SS1	-	-	-	-	EVENT_OUT
PB12	-	I2C2_SMBA	USART3_CK	SPI2_NSS	TIM1_BKIN	-	-	TIM5_ETR	–	-	-	-	-	-	SPI2_NSS	EVENT_OUT
PB13	-	-	USART3_CTS	SPI2_SCK	TIM1_CH1N	-	-	-	–	-	-	-	-	-	SPI2_MOSI	EVENT_OUT
PB14	-	-	USART3_RTS	SPI2_MISO	TIM1_CH2N	-	-	-	TIM12_CH1	-	-	-	-	-	-	EVENT_OUT
PB15	-	-	-	SPI2_MOSI	TIM1_CH3N	-	-	-	TIM12_CH2	-	-	-	-	-	SPI2_MOSI	EVENT_OUT

3.3. Alternate functions selected through GPIOC_AFR registers for port C

Table 3-5 Port C alternate function mapping

PortC	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PC1	-	-	-	-	-	-	-	-	-	-	ESMC_IO4	-	-	-	-	EVENT_OUT
PC2	-	-	-	-	-	-	-	-	-	-	ESMC_IO5	-	-	-	-	EVENT_OUT
PC3	-	-	-	-	-	-	-	-	-	-	ESMC_IO6	-	-	-	-	EVENT_OUT
PC4	-	-	-	-	-	-	-	-	-	-	ESMC_IO7	-	-	-	-	EVENT_OUT
PC5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	I2S1_MCK	EVENT_OUT
PC6	-	USART4_CK	-	-	-	TIM8_CH1	TIM3_CH1	-	-	-	-	SDIO_D6	-	-	I2S2_MCK	EVENT_OUT
PC7	-	USART4_CTS	-	-	-	TIM8_CH2	TIM3_CH2	-	-	-	-	SDIO_D7	-	-	I2S3_MCK	EVENT_OUT

PortC	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC8	-	USART4_RTS	-	-	-	TIM8_CH3	TIM3_CH3	-	-	-	-	SDIO_D0	-	-	-	EVENT_OUT
PC9	-	-	-	-	-	TIM8_CH4	TIM3_CH4	-	-	-	-	SDIO_D1	-	-	-	EVENT_OUT
PC10	-	USART4_TX	USART3_TX	-	-	-	-	-	-	-	-	SDIO_D2	-	-	SPI_SCK	EVENT_OUT
PC11	-	USART4_RX	USART3_RX	-	-	-	-	-	-	-	-	SDIO_D3	-	-	SPI_NSS	EVENT_OUT
PC12	-	USART5_TX	USART3_CK	-	-	-	-	-	-	-	-	SDIO_CK	-	-	SPI_MOSI	EVENT_OUT
PC13	-	-	-	-	-	-	-	-	-	-	-	–	-	-	–	EVENT_OUT
PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT

3.4. Alternate functions selected through GPIOD_AFR registers for port D

Table 3-6 Port D alternate function mapping

PortD	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0	-	–	-	-	-	-	-	-	-	-	CAN_RX	-	-	-	-	EVENT_OUT
PD1	-	–	-	-	-	-	-	-	-	-	CAN_TX	-	-	-	-	EVENT_OUT
PD2	-	USART5_RX	-	-	-	-	TIM3_ETR	-	-	-	-	SDIO_CMD	-	-	-	EVENT_OUT
PD3	-	USART5_CK	USART2_CTS	-	-	-	-	-	-	-	ESMC_SS2	-	-	-	-	EVENT_OUT
PD4	-	USART5_CTS	USART2_RTS	-	-	-	-	-	-	-	ESMC_IO4	-	-	-	-	EVENT_OUT
PD5	-	USART5_RTS	USART2_TX	-	-	-	-	-	-	-	ESMC_IO5	-	-	-	-	EVENT_OUT
PD6	-	-	USART2_RX	-	-	-	-	-	-	-	ESMC_IO6	-	-	-	-	EVENT_OUT
PD7	-	-	USART2_CK	-	-	-	-	-	-	-	ESMC_IO7	-	-	-	-	EVENT_OUT
PD8	-	-	USART3_TX	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PD9	-	-	USART3_RX	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PD10	-	-	USART3_CK	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PD11	-	-	USART3_CTS	-	-	-	-	TIM5_ETR	-	-	-	-	-	-	-	EVENT_OUT
PD12	-	-	USART3_RTS	-	-	-	TIM4_CH1	-	-	-	-	-	-	-	-	EVENT_OUT
PD13	-	-	-	-	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	EVENT_OUT
PD14	-	-	-	-	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	EVENT_OUT
PD15	-	-	-	-	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	EVENT_OUT

3.5. Alternate functions selected through GPIOA_AFR registers for port E

Table 3-7 Port E alternate function mapping

PortE	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0	-	-	-	-	-	-	TIM4_ETR	-	-	-	-	-	-	-	-	EVENT_OUT
PE1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PE2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PE3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PE4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PE5	-	-	-	-	-	-	-	-	TIM9_CH1	-	-	-	-	-	-	EVENT_OUT
PE6	-	-	-	-	-	-	-	-	TIM9_CH2	-	-	-	-	-	-	EVENT_OUT
PE7	-	-	-	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PE8	-	-	-	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PE9	-	-	-	-	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	EVENT_OUT
PE10	-	-	-	-	TIM1_CH2N	-	-	-	-	-	ESMC_CLK	-	-	-	-	EVENT_OUT
PE11	-	-	-	-	TIM1_CH2	-	-	-	-	-	ESMC_SS3	-	-	-	-	EVENT_OUT
PE12	-	-	-	-	TIM1_CH3N	-	-	-	-	-	ESMC_IO0	-	-	-	-	EVENT_OUT
PE13	-	-	-	-	TIM1_CH3	-	-	-	-	-	ESMC_IO1	-	-	-	-	EVENT_OUT
PE14	-	-	-	-	TIM1_CH4	-	-	-	-	-	ESMC_IO2	-	-	-	-	EVENT_OUT
PE15	-	-	-	-	TIM1_BKIN	-	-	-	-	-	ESMC_IO3	-	-	-	-	EVENT_OUT

4. Memory mapping

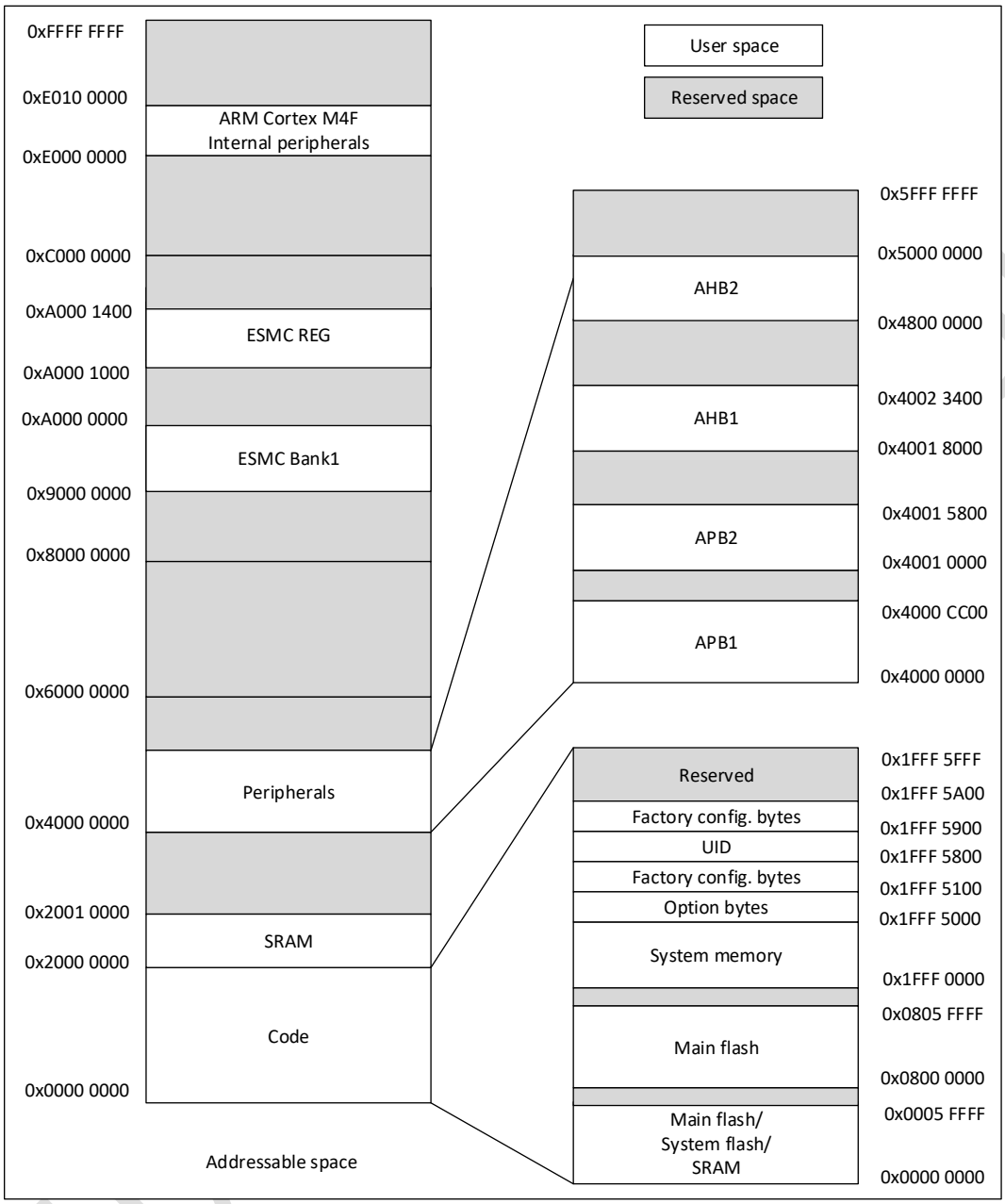


Figure 4-1 Memory map

Table 4-1 Memory boundary address

Type	Boundary address	Size	Memory area	Description
SRAM	0x2001 0000-0x3FFF FFFF	-	Reserved	1. When the CPU reads and writes this space, a Response error is generated, and then a HardFault exception is entered. 2. A TEIF status bit is generated when DMA accesses
	0x2000 0000-0x2000 FFFF	64 KB	SRAM	If the hardware power-on configuration SRAM is 64 KB, the SRAM address space is 0x2000 0000-0x2000 FFFF
Code	0x1FFF 5A00-0x1FFF 5FFF	-	Reserved	-
	0x1FFF 5900-0x1FFF 59FF	256 Bytes	Factory config. bytes	-
	0x1FFF 5800-0x1FFF 58FF	256 Bytes	UID bytes	Unique ID
	0x1FFF 5700-0x1FFF 57FF	256 Bytes	Factory config. bytes	-
	0x1FFF 5600-0x1FFF 56FF	256 Bytes	HSI8M Trim	-
	0x1FFF 5500-0x1FFF 55FF	256 Bytes	Factory config. bytes	-
	0x1FFF 5400-0x1FFF 54FF	256 Bytes	Factory config. bytes	-
	0x1FFF 5300-0x1FFF 53FF	256 Bytes	Factory config. bytes	-
	0x1FFF 5200-0x1FFF 52FF	256 Bytes	Factory config. bytes	-
	0x1FFF 5100-0x1FFF 51FF	256 Bytes	Factory config. bytes	-
	0x1FFF 5000-0x1FFF 50FF	256 Bytes	Option bytes	Software and hardware option bytes information
	0x1FFF 0000-0x1FFF 4FFF	24 KB	System memory	Store boot loader
	0x0806 0000-0x1FFE FFFF	-	Reserved	-
	0x0800 0000-0x0805 FFFF	384 KB	Main flash memory	-
	0x0006 0000-0x07FF FFFF	8 MB	Reserved	1. When the CPU reads and writes this space, a Response error is generated, and then a HardFault exception is entered. 2. A TEIF status bit is generated when DMA accesses
	0x0000 0000-0x0005 FFFF	384 KB	Depending on the Boot configuration selection: 1) Main flash memory System memory 3) SRAM	-

1. The address is marked as Reserved, which cannot be written, read as 0, and a response error is generated.

Table 4-2 Peripheral register address

Memory boundary address	Peripherals	Bus
0xA000 1000 - 0xA000 13FF	ESMC	AHB
0x4002 3400 - 0x5FFF FFFF	Reserved	AHB2
0x4800 1000 - 0x4800 13FF	GPIOE	
0x4800 0C00 - 0x4800 0FFF	GPIOD	
0x4800 0800 - 0x4800 0BFF	GPIOC	
0x4800 0400 - 0x4800 07FF	GPIOB	
0x4800 0000 - 0x4800 03FF	GPIOA	
0x4002 3400 - 0x47FF FFFF	Reserved	AHB1
0x4002 3000 - 0x4002 33FF	CRC	
0x4002 2400 - 0x4002 2FFF	Reserved	
0x4002 2000 - 0x4002 23FF	FMC	
0x4002 1400 - 0x4002 1FFF	Reserved	
0x4002 1000 - 0x4002 13FF	RCC	
0x4002 0800 - 0x4002 0FFF	Reserved	
0x4002 0400 - 0x4002 07FF	DMA2	
0x4002 0000 - 0x4002 03FF	DMA1	
0x4001 8400 - 0x4001 FFFF	Reserved	
0x4001 8000 - 0x4001 83FF	SDIO	
0x4001 5800 - 0x4001 7FFF	DBG	APB2
0x4001 5400 - 0x4001 57FF	TIMER11	
0x4001 5000 - 0x4001 53FF	TIMER10	
0x4001 4C00 - 0x4001 4FFF	TIMER9	
0x4001 4000 - 0x4001 4BFF	Reserved	
0x4001 3C00 - 0x4001 3FFF	ADC3	
0x4001 3800 - 0x4001 3BFF	USART1	
0x4001 3400 - 0x4001 37FF	TIMER8	
0x4001 3000 - 0x4001 33FF	SPI1/I^2S	
0x4001 2C00 - 0x4001 2FFF	TIMER1	
0x4001 2800 - 0x4001 2BFF	ADC2	
0x4001 2400 - 0x4001 27FF	ADC1	
0x4001 0800 - 0x4001 23FF	Reserved	
0x4001 0400 - 0x4001 07FF	EXTI	
0x4001 0000 - 0x4001 03FF	SYSCFG	
0x4000 CC00 - 0x4000 FFFF	Reserved	APB1
0x4000 C800 - 0x4000 CBFF	CTC	
0x4000 7800 - 0x4000 C7FF	Reserved	
0x4000 7400 - 0x4000 77FF	DAC	
0x4000 7400 - 0x4000 77FF	Reserved	
0x4000 7000 - 0x4000 73FF	PWR	

Memory boundary address	Peripherals	Bus
0x4000 6C00 - 0x4000 6FFF	BKP	
0x4000 6800 - 0x4000 6BFF	Reserved	
0x4000 6400 - 0x4000 67FF	CANFD	
0x4000 6000 - 0x4000 63FF	USBD/CANFD share 512 bytes of SRAM	
0x4000 5C00 - 0x4000 5FFF	USBD	
0x4000 5800 - 0x4000 5BFF	I2C2	
0x4000 5400 - 0x4000 57FF	I2C1	
0x4000 5000 - 0x4000 53FF	UASRT5	
0x4000 4C00 - 0x4000 4FFF	UASRT4	
0x4000 4800 - 0x4000 4BFF	USART3	
0x4000 4400 - 0x4000 47FF	USART2	
0x4000 4000 - 0x4000 43FF	Reserved	
0x4000 3C00 - 0x4000 3FFF	SPI3/I^2S	
0x4000 3800 - 0x4000 3BFF	SPI2/I^2S	
0x4000 3400 - 0x4000 37FF	Reserved	
0x4000 3000 - 0x4000 33FF	IWDG	
0x4000 2C00 - 0x4000 2FFF	WWDG	
0x4000 2800 - 0x4000 2BFF	RTC	
0x4000 2400 - 0x4000 27FF	Reserved	
0x4000 2000 - 0x4000 23FF	TIMER14	
0x4000 1C00 - 0x4000 1FFF	TIMER13	
0x4000 1800 - 0x4000 1BFF	TIMER12	
0x4000 1400 - 0x4000 17FF	TIMER7	
0x4000 1000 - 0x4000 13FF	TIMER6	
0x4000 0C00 - 0x4000 0FFF	TIMER5	
0x4000 0800 - 0x4000 0BFF	TIMER4	
0x4000 0400 - 0x4000 07FF	TIMER3	
0x4000 0000 - 0x4000 03FF	TIMER2	

5. Electrical characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25 °C and T_A=T_A(max) (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization,the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 σ).

5.1.2. Typical values

Unless otherwise specified, typical data is based on T_A=25°C and V_{CC}= 3.3 V. These data are for design guidance only and have not been tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2 σ).

5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics(1)

Symbol	Descriptions	Min	Max	Unit
V_{CC}-V_{SS}	External supply voltage (including V_{CC}, V_{CCA}, V_{BAT}, V_{REF+}) (1)	-0.3	4.0	V
V_{IN}(2)	FT_xx, NRST I/O input voltage	V_{SS}-0.3	5.5	
	TT_xx I/O input voltage	V_{SS}-0.3	4.0	
|DV_{CCx}|	Voltage variation between different V_{CC} pins	-	50	mV
|V_{SSX} -V_{SS}|	Voltage variation between different ground pins	-	50	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. Maximum V_{IN} must always follow allowable maximum injection current limits as per the table.

Table 5-2 Current characteristics

Symbol	Descriptions	Max	Unit
ΣI_{VCC}	Total current into sum of all V_{CC}/V_{CCA} power lines (source)(1)	180	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	180	
$\Sigma I_{IO(PIN)}$(2)	Total output current sunk by sum of all I/Os and control pins	170	
	Total output current sourced by sum of all I/Os and control pins	170	
I_{IO}(2)	Output current sunk by any I/O and control pin	30	
	Output current sourced by any I/Os and control pin(3)	30	
$I_{INJ(PIN)}$	Injected current on FT_xx I/O(4)	-5/+0	
	Injected current on any other pin(5)	± 5	
$\Sigma I_{INJ(PIN)}$(7)	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. Main power V_{CC} and ground V_{SS} pins must always be connected to the external power supply, in the permitted range.
2. These I/O types refer to the terms and symbols defined by pins.
3. PC13, PC14, PC15 pins are not included because they are powered by power switch. The current sourced

capacity is limited to 3 mA.
4. Negative injection disturbs the analog performance of the device.
5. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
6. A positive injection is induced by $V_{IN}>V_{CCA}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
7. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 5-3 Thermal characteristics

Symbol	Descriptions	Max	Unit
T_{STG}	Storage temperature range	-65 to 150	℃
T_J	Maximum junction temperature	150	℃

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	AHB clock frequency	-	0	144	MHz
f_{PCLK1}	APB1 clock frequency	-	0	144	
f_{PCLK2}	APB2 clock frequency	-	0	144	
V_{CC}	Operating voltage	-	1.8	3.6	V
V_{CCA}	Operating voltage of analog circuit	Must be the same potential as V_{CC}	1.8	3.6	V
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	FT_xx, NRST I/O input voltage	-	V_{SS} - 0.3	5.5	V
	TT_xx I/O input voltage	-	V_{SS} - 0.3	3.6	
T_A	Ambient temperature	-	-40	105	℃
T_J	Junction temperature	-	-40	110	℃

5.3.2. Operating conditions at power-on / power-down

Table 5-5 Operating conditions at power-on / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise rate	-	50	∞	μs/V
	V_{CC} fall rate	V_{CC} and V_{BAT} drop synchronously	20	∞	
		V_{CC} drops and V_{BAT} holds	100	∞	

5.3.3. Reset and power control block characteristics

Table 5-6 Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	PVD threshold	PLS[2:0]=000 (Rising edge)	1.7	1.8	1.9	V
		PLS[2:0]=000 (Falling edge)	1.6	1.7	1.8	
		PLS[2:0]=001 (Rising edge)	1.9	2	2.1	
		PLS[2:0]=001 (Falling edge)	1.8	1.9	2	
		PLS[2:0]=010 (Rising edge)	2.1	2.2	2.3	
		PLS[2:0]=010 (Falling edge)	2	2.1	2.2	
		PLS[2:0]=011 (Rising edge)	2.3	2.4	2.5	
		PLS[2:0]=011 (Falling edge)	2.2	2.3	2.4	
		PLS[2:0]=100 (Rising edge)	2.5	2.6	2.7	
		PLS[2:0]=100 (Falling edge)	2.4	2.5	2.6	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		PLS[2:0]=101 (Rising edge)	2.7	2.8	2.9	
		PLS[2:0]=101 (Falling edge)	2.6	2.7	2.8	
		PLS[2:0]=110 (Rising edge)	2.9	3	3.1.	
		PLS[2:0]=110 (Falling edge)	2.8	2.9	3	
		PLS[2:0]=111 (Rising edge)	3.1.	3.2	3.3	
		PLS[2:0]=111 (Falling edge)	3	3.1.	3.2	
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	falling edge	1.58	1.63	1.68	V
		rising edge	1.56	1.61	1.66	
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	20	-	mV
$t_{RSTTEMPO}$(2)	POR reset temporization	-	1	2.5	4.5	ms

1. Guaranteed by design, not tested in production.
2. The reset temporization is measured from the power-on (POR reset or wake-up from V_{BAT}) to the instant when the first instruction is read by the user application code.

5.3.4. Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. All the run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{CC} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 28 MHz, 1 wait state from 28 to 60 MHz, 3 wait states from 60 to 90 MHz, 4 wait states from 90 to 120 MHz, 5 wait states from 120 to 140 MHz, and 6 wait states beyond 140 MHz).
- The maximum values are obtained for V_{CC} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{CC} = 3.3 V unless otherwise specified.
- Command prefetch function is turned on. When the peripheral is turned on: $f_{PCLK1} = f_{HCLK}$.

Note: The command prefetch function must be set before setting the clock and bus frequency division.

Table 5-7 Current consumption in Run mode (Flash)

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max		Unit
				T_A = 25 ℃	TA = 85 °C	TA = 105 °C	
I_{CC}	Supply current in Run mode	All Peripherals enabled	144 MHz	25.60	-	-	mA
			96 MHz	18.24	-	-	
			64 MHz	13.20	-	-	
			48 MHz	11.32	-	-	
			32 MHz	8.31	-	-	
			16 MHz	5.43	-	-	
			8 MHz	1.99	-	-	
		All Peripherals disabled	144 MHz	15.09	-	-	
			96 MHz	11.07	-	-	
			64 MHz	8.37	-	-	
			48 MHz	7.50	-	-	
			32 MHz	5.71	-	-	
			16 MHz	3.91	-	-	
			8 MHz	1.35	-	-	

Table 5-8 Current consumption in Run mode (SRAM)

Symbol	Parameter	Conditions[3]	f_{HCLK}	Typ	Max[1]		Unit
				T_A = 25 ℃	TA = 85 °C	TA = 105 °C	
I_{CC}	Supply current in Run mode	All Peripherals[2] enabled	144 MHz	24.61	-	-	mA
			96 MHz	17.55	-	-	
			64 MHz	12.78	-	-	
			48 MHz	10.83	-	-	
			32 MHz	7.99	-	-	
			16 MHz	3.92	-	-	
			8 MHz	2.09	-	-	
		All Peripherals[2] disabled	144 MHz	14.39	-	-	
			96 MHz	10.68	-	-	
			64 MHz	8.07	-	-	
			48 MHz	7.33	-	-	
			32 MHz	5.65	-	-	
			16 MHz	2.68	-	-	
			8 MHz	1.49	-	-	

1. Evaluated by characterization, not tested in production.
2. The external clock is 16 MHz and the PLL is enabled when f_{HCLK} > 8 MHz.
3. 8 MHz is the internal HSI clock.

Table 5-9 Current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ	Max[1]		Unit
				T_A = 25 ℃	TA = 85 ℃	TA = 105 ℃	
I_{CC}	Supply current in Sleep mode	All Peripherals enabled	144 MHz	19.37	-	-	mA
			96 MHz	14.07	-	-	
			64 MHz	10.44	-	-	
			48 MHz	7.21	-	-	
			32 MHz	5.45	-	-	
			16 MHz	3.32	-	-	
			8 MHz	1.82	-	-	
		All Peripherals disabled	144 MHz	6.60	-	-	
			96 MHz	4.98	-	-	
			64 MHz	3.95	-	-	
			48 MHz	3.41	-	-	
			32 MHz	2.86	-	-	
			16 MHz	1.95	-	-	
			8 MHz	1.07	-	-	

1. Data based on characterization results, not tested in production.

Table 5-10 Current consumption in Stop and Standby mode

Symbol	Parameter	Conditions	Typ			Max[1]		Unit
			V_{CC}/V_{BAT} = 2.0 V	V_{CC}/V_{BAT} = 2.4 V	V_{CC}/V_{BAT} = 3.3 V	T_A = 85 ℃	T_A = 105 ℃	
I_{CC}	Supply current in Stop mode	In LDO Run mode, internal high-speed oscillator, internal low-speed oscillator and high-speed oscillator OFF.	432	-	-	-	-	µA
		In LDO low power mode, internal high-	370	-	-	-	-	

Symbol	Parameter	Conditions	Typ			Max(1)		Unit
			V_{CC}/V_{BAT} = 2.0 V	V_{CC}/V_{BAT} = 2.4 V	V_{CC}/V_{BAT} = 3.3 V	T_A = 85 ℃	T_A = 105 ℃	
		speed oscillator, internal low-speed oscillator and high-speed oscillator OFF.						
	Supply current in Standby mode	Internal low speed oscillator and IWDG ON	4.8	-	-	-	-	
		Internal low speed oscillator ON, IWDG OFF	4.8	-	-	-	-	
		Internal low speed RC oscillator and IWDG OFF, low speed oscillator and RTC OFF	4.7	-	-	-	-	
I_{CC_VBAT}	Backup domain supply current	Low speed oscillator and RTC off	4.7	-	-	-	-	
		Low speed oscillator and RTC on	4.8	-	-	-	-	

1. Evaluated by characterization, not tested in production.

5.3.5. Wakeup time from low-power mode

Table 5-11 Low power mode wake-up time(2)(3)

Symbol	Parameter	Typ(3)	Unit
$t_{WUSLEEP}$(1)	Wake up from Sleep mode	6	CPU cycles
t_{WUSTOP}(1)	Wake up from Stop mode (LDO run mode)	6.88	μs
	Wake up from Stop mode (LDO low power mode)	10.66	
$t_{WUSTDBY}$(1)	Wake up from Standby mode	79.50	μs

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data based on characterization results, not tested in production.
3. Data are based on HSI 8 M conditions.

5.3.6. External clock source characteristics

5.3.6.1. High-speed external clock generated from an external source

In bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the device stops working, the corresponding I/O is used as a standard GPIO.

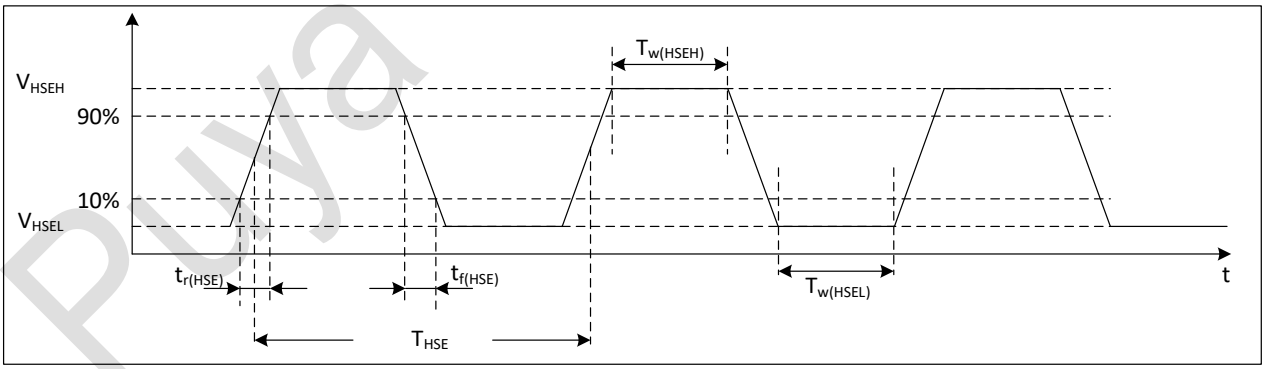


Figure 5-1 High-speed external clock timing diagram

Table 5-12 High-speed external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency(1)	-	1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7V_{CC}	-	V_{CC}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	0.3V_{CC}	
$t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ /$t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{CC}$	-	-	±1	μA

1. Guaranteed by design, not tested in production.

5.3.6.2. Low-speed external clock generated from an external source

In the bypass mode of LSE (the LSEBYP of RCC_BDCR is set), the low-speed start-up circuit in the chip stops working, and the corresponding I/O is used as a standard GPIO.

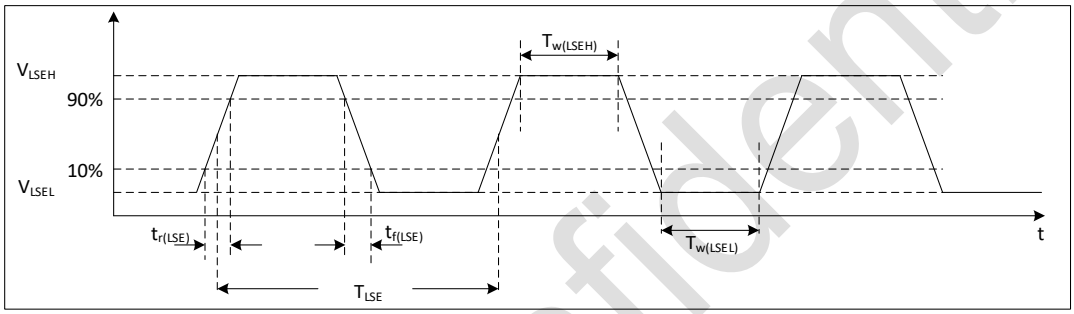


Figure 5-2 Low-speed external clock timing diagram

Table 5-13 Low-speed external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		0.7V_{CC}	-	V_{CC}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	0.3V_{CC}	
$t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ /$t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{CC}$	-	-	±1	μA

1. Guaranteed by design, not tested in production.

5.3.6.3. High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with 4 to 32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-14 HSE oscillator characteristics

Symbol	Parameter	Conditions		Min	Typ(1)	Max	Unit
f_{OSC_IN}	Oscillator frequency	-		4	8	32	MHz
R_F	Feedback resistor	-		-	200	-	kΩ
I_{CC}	HSE current consumption	C_L=12 pF@32 MHz，HSE_DRV[1:0]=01		-	-	1	mA
g_m	Maximum critical crystal gm	Startup	HSE_DRV[1:0]=00	3.5	-	-	mA/V
			HSE_DRV[1:0]=01	5	-	-	
			HSE_DRV[1:0]=10	7.5	-	-	
			HSE_DRV[1:0]=11	10	-	-	
$t_{SU(HSE)}$(2)	Startup time	V_{CC} is stable		-	0.7	-	ms

1. Evaluated by characterization, not tested in production.
2. The relatively low RF resistance values provide better protection due to induced leakage and changes in bias conditions when used in humid environments. However, if the MCU is used in harsh humidity conditions, it is recommended to take this parameter into account in design.

5.3.6.4. Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-15 LSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
RF	Feedback resistor	-	-	5	-	MΩ
I_{CC}	LSE current consumption	LSE_DRV_VBKP[1:0]=00	-	500	-	nA
		LSE_DRV_VBKP[1:0]=01	-	630	-	nA
		LSE_DRV_VBKP[1:0]=10	-	250	-	nA
		LSE_DRV_VBKP[1:0]=11	-	315	-	nA
g_m	Maximum critical crystal gm	LSE_DRV_VBKP[1:0]=00	8.5	-	-	μA/V
		LSE_DRV_VBKP[1:0]=01	13.5	-	-	μA/V
		LSE_DRV_VBKP[1:0]=10	2.5	-	-	μA/V
		LSE_DRV_VBKP[1:0]=11	3.75	-	-	μA/V
$t_{SU(LSE)}$(2)	Startup time	V_{CC} is stable	-	0.5	-	s

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.7. High-speed internal (HSI) RC oscillator

Table 5-16 High-speed internal (HSI 8) RC oscillator characteristics

Symbol	Parameter	Conditions		Min(1)	Typ(1)	Max(1)	Unit
f_{HSI}	Frequency	-		7.92	8	8.08	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	HSI oscillator accuracy	Using the RCC_CR register to adjust		-	0.5	1(2)	%
		Factory calibration	T_A = -10 to 85 °C	-2.5	-	2.5	%
			T_A = -40 to 105 °C	-3.0	-	3.0	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-		1	-	2	μs
$I_{CC(HSI)}$(2)	HSI oscillator power consumption	-		-	80	150	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

Table 5-17 High-speed internal (HSI 48) RC oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI48 frequency	V_{CC}=3.3 V, T_A = 25 °C	47.52	48	48.48	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
$\Delta_{Temp(HSI)}$	HSI 48M frequency drift over temperature	T_A = 0 to 85 °C	-3.0	-	3.0	%
		T_A = -40 to 105 °C	-3.5	-	3.5	
$t_{su(HSI)}$(2)	HSI48 oscillator startup time	-	-	25	-	μs
$I_{CC(HSI)}$(2)	HSI48 oscillator power consumption	48 MHz	-	360	-	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.8. Low-speed internal (LSI) RC oscillator

Table 5-18 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{CC} = 3.3 V, T_A = 25 °C	38.6	40	41.4	kHz
		V_{CC} = 1.8 to 3.6 V, T_A = -40 to 105 °C	30	40	50	kHz
$t_{su(LSI)}$(1)	LSI oscillator startup time	-	-	-	85	μs
$I_{CC(LSI)}$(1)	LSI oscillator power consumption	-	-	0.2	0.3	μA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.9. Phase locked loop (PLL) characteristics

Table 5-19 PLL characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock	8	24	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	48	-	144	MHz
t_{LOCK}	PLL lock time	-	25	550	μs
Jitter	Jitter	-	-	180	ps

1. Guaranteed by design, not tested in production.

5.3.10. Memory characteristics

Table 5-20 Memory characteristics(2)

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max	Unit
N_{END}	Endurance	T_A = -40 to 85 °C	100	-	-	kcycles
		T_A = 85 to 105 °C	10	-	-	
t_{RET}	Data retention	1 kcycle at T_A = 55 ℃	20	-	-	years
		1 kcycle at T_A = 85 ℃	15	-	-	
		1 kcycle at T_A = 105 ℃	10	-	-	
		10 kcycles at T_A = 55 ℃	10	-	-	
t_{PROG}	Page programming time	T_A = -40 to 105 °C	-	1.5	-	ms
t_{ERASE}	Page erase time	T_A = -40 to 105 °C	-	5	-	ms
t_{MERASE}	Mass erase time	T_A = -40 to 105 °C	-	5	-	ms

1. Guaranteed by design, not tested in production.
2. During Flash erase/write operations, code cannot be executed from SRAM, otherwise the CPU will stop functioning.

5.3.11. ESD & LU characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Table 5-21 ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A= 25 °C; JESD22-A114	-	-	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charged device model)	T_A= 25 °C; JESD22-C101	-	-	1000	V
LU	Overcurrent test	T_A= 25 °C; JESD78A	-	-	± 200	mA
	Overvoltage test		-	-	5.4	V

5.3.12. I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{CC} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

An out of range parameter indicates the failure: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins, or other functional failure (for example reset, oscillator frequency deviation).

Table 5-22 I/O current injection susceptibility

Symbol	Descriptions	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PC13, PC14 and PC15	0	0	mA
	Injected current on FT_xx I/O	-5	0	
	Injected current on any other pin	-5	5	

5.3.13. EFT characteristics

Table 5-23 EFT characteristics

Symbol	Parameter	Conditions	Grade
EFT to Power	-	IEC61000-4-4	4 A

5.3.14. I/O port characteristics

Table 5-24 IO port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TT_xx I/O，1.8 V≤V_{CC}≤ 3.6 V	-0.3	-	0.35*V_{CC}-0.06	V
		FT_xx I/O，1.8 V≤V_{CC}≤ 3.6 V	-0.3	-	0.4*V_{CC}-0.04	
V_{IH}	Input high level voltage	TT_xx I/O，1.8 V≤V_{CC}≤ 3.6 V	0.6*V_{CC}+0.14	-	V_{CC}+0.3	V
		FT_xx I/O，1.8 V≤V_{CC}≤ 3.6 V	0.45*V_{CC}+0.23	-	5.5	
V_{hys}(1)	Schmitt trigger hysteresis	1.8 V≤V_{CC}≤ 3.6 V	-	50	-	mV

I_{lkg}(2)	Input leakage current	TT_xxI/O, V_{SS}≤V_{IN}≤V_{CC}	-	-	-1	μA
		FT_xx I/O, V_{IN} =5 V	-	-	3	
R_{PU}(3)	Internal Pull-up Resistor	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}(3)	Internal Pull-down Resistor	V_{IN} = V_{CC}	30	40	50	kΩ
CIO	Pin capacitance	-	-	5	-	pF
$t_{ns(EXIT)}$(1)	Input filter width	ENI=1, ENS=1	3	5	10	ns
$t_{ns(I2C)}$(1)	I^2C input filter width	ENI=1, EIIC=1	50	140	250	ns
$t_{ns(NRST)}$(1)	NRST input filter width	ENI=1, EIIC=1	100	18	300	ns

1. Guaranteed by design, not tested in production.
2. If there is reverse current pouring in adjacent pins, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are designed to be a real resistor in series with a switchable PMOS/NMOS.

Output driving current

The GPIOs (general-purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15, which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins, which can drive current must be limited to respect the absolute maximum rating.

- The sum of the currents sourced by all the I/Os on V_{CC}, plus the maximum Run consumption of the MCU sourced on V_{CC}, cannot exceed the absolute maximum rating I_{VCC}.
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS}.

Output voltage

Unless otherwise specified, the parameters given in table below are derived from tests performed under ambient temperature and V_{CC} supply voltage conditions.

Table 5-25 Output voltage characteristics(3)

Symbol	Parameter	Conditions	Min	Typ	Max(2)	Unit
V_{OL}(1)	Output low level voltage for eight I/O pins	2.7 V≤V_{CC}≤ 3.6 V，I_{IO} = +8 mA	-	-	0.4	V
		2.7 V≤V_{CC}≤ 3.6 V，I_{IO} = +20 mA	-	-	1.3	
		1.8 V≤V_{CC}≤ 2.7 V，I_{IO} = +6 mA	-	-	0.4	
V_{OH}(1)	Output high level voltage for eight I/O pins	2.7 V≤V_{CC}≤ 3.6 V，I_{IO} = +8 mA	V_{CC}-0.4	-	-	
		2.7 V≤V_{CC}≤ 3.6 V，I_{IO} = +20 mA	V_{CC}-1.3	-	-	
		1.8 V≤V_{CC}≤ 2.7 V，I_{IO} = +6 mA	V_{CC}-0.4	-	-	

1. These I/O types refer to the terms and symbols defined by pins.
2. Data based on characterization results, not tested in production.
3. The combined maximum current across all output pins (including contributions from both V_{OL} and V_{OH} states) must not exceed the $\Sigma I_{IO(PIN)}$ maximum rating specified in Table 5-2 Current Characteristics.

5.3.15. ADC characteristics

Table 5-26 ADC characteristics

Symbol	Parameter	Conditions(4)	Min	Typ	Max	Unit
V_{CCA}(3)	Supply voltage	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8	-	V_{CCA}	V
I_{VCCA}	V_{CCA} pin current	f_{ADC} = 16 MHz	-	280	370(1)	μA
I_{VREF}	V_{REF} pin voltage	f_{ADC} = 16 MHz	-	8	10(1)	μA
f_{ADC}	ADC clock frequency	-	0.8	-	16	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	-	-	30.9	kΩ

Symbol	Parameter	Conditions(4)	Min	Typ	Max	Unit
R_{ADC}(2)	Sampling switch resistance	-	-	-	1.6	kΩ
C_{ADC}(2)	Internal sampling and holding capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 16 MHz	5.6875 to 8.75			μs
		-	91 (1 clk sampling time) to 140 (8 clk sampling time)			$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 16 MHz	0.218	-	14.968	μs
		-	3.5	-	239.5	$1/f_{ADC}$
t_{samp_setup}	Sampling time for internal channels	-	20	-	-	μs
t_{STAB}(2)	Power-on Stabilization time	-	0	0	1	μs
t_{CONV}(2)	Total conversion time	f_{ADC} = 16 MHz	1	-	15.75	μs
		-	16 to 252 (sampling ts + successive approximation 12.5)			$1/f_{ADC}$

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. For some package types, V_{REF+} can be internally connected to V_{CCA}, and V_{REF-} can be internally connected to V_{SSA}. For details, please refer to the pin definitions.
4. When using external triggering, an additional delay of $1/f_{PCLK2}$ is required.
   a) $R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$
   b) The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution).

Table 5-27 R_{AIN} max for f_{ADC} = 16 MHz(1)

T_s (sampling cycle)	t_s (μs)	R_{AIN} max (kΩ)
3.5	0.21	0.3
5.5	0.34	1.9
7.5	0.46	3.5
13.5	0.84	8.3
28.5	1.78	20.4
41.5	2.59	30.9
134.5	8.41	NA
239.5	15.96	NA

1. Guaranteed by design, not tested in production.

Table 5-28 ADC accuracy(1)(2)(3)(4)

Symbol	Parameter	Parameter conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	1.8 V < V_{CCA}=V_{REF+} < 3.6 V; f_{ADC} = 16 MHz; fs ≤ 1 MSps; T_A = entire range	7.5	15	LSB
EO	Offset error	V_{CCA}=V_{REF+} = 3.3 V; f_{ADC} = 16 MHz; fs ≤ 1 MSps T_A = entire range	2	4	LSB
		1.8 V < V_{CCA}=V_{REF+} < 3.6 V; f_{ADC} = 16 MHz; fs ≤ 1 MSps T_A = entire range	2	6	
EG	Gain error	V_{CCA}=V_{REF+} = 3.3 V; f_{ADC} = 16 MHz; fs ≤ 1 MSps T_A = entire range	4	5	LSB
		1.8 V < V_{CCA}=V_{REF+} < 3.6 V; f_{ADC} = 16 MHz; fs ≤ 1 MSps T_A = entire range	4	8	

Symbol	Parameter	Parameter conditions	Typ	Max(3)	Unit
ED	Differential linearity error	1.8 V < V_{CCA}=V_{REF+} < 3.6 V; f_{ADC} = 16 MHz; fs ≤ 1 MSps T_A = entire range	1.2	1.5	LSB
EL	Integral linearity	1.8 V < V_{CCA}=V_{REF+} < 3.6 V; f_{ADC} = 16 MHz; fs ≤ 1 MSps T_A = entire range	4	6	LSB

1. Data based on characterization results, not tested in production.
2. ADC accuracy values are measured after internal calibration.
3. ADC accuracy and reverse injection current: Reverse current injection on any standard analog input pin should be avoided, as it will significantly reduce the conversion accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to the standard analog input pins where reverse injection current may occur. If the forward injection current is within the $I_{INJ (PIN)}$ and $\Sigma I_{INJ (PIN)}$ ranges given in I/O current injection characteristics, it will not affect the ADC accuracy.
4. Evaluated by characterization, not tested in production.

5.3.16. DAC characteristics

Table 5-29 DAC characteristics (PA4 pin)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CCA}	Analog power supply	2.2	-	3.6	V	
V_{REF+}	Positive reference voltage	2.2	-	3.6	V	V_{REF+} ≤ V_{CCA}
V_{SSA}	Ground	0	-	0	V	
R_{LOAD}(1)	Load connected to V_{SSA}	5	-	-	kΩ	
	Load connected to V_{CCA}	15	-	-	kΩ	
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	The minimum resistive load between DAC_VOUT and V_{SS} to have a 1% accuracy is 1.5 MΩ when the buffer is OFF.
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (When the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{CCA}-0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5		mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-		V_{REF+} -10 mV	V	
I_{CC_VREF+}	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-		380	μA	With no load, worst code (0x0E4) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs.
I_{CCA}	DAC DC V_{CCA} current consumption in quiescent mode(2)	-		380	μA	With no load, middle code (0x800) on the inputs
		-		480	μA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(3)		-	±1.5	-	LSB	Given for the DAC in 8-bit configuration

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Differential non linearity (Difference between two consecutive code-1LSB)	-	±2		LSB	Given for the DAC in 12-bit configuration
INL(2)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	±1.5	-	LSB	Given for the DAC in 8-bit configuration
		-	±2		LSB	Given for the DAC in 12-bit configuration
Offset(2)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	±12	LSB	Given for the DAC in 12-bit configuration V_{REF+} = 3.3 V
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(2)	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(2)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	C_{LOAD} ≤ 50pF, R_{LOAD} ≥ 5 kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	C_{LOAD} ≤ 50pF, R_{LOAD} ≥ 5 kΩ
t_{WAKEUP}(2)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ input code between lowest and highest possible ones.
PSRR+(1)	Power supply rejection ratio (to V_{CCA}) (static DC measurement)	-	-67	-40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design, not tested in production.
2. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.

Table 5-30 DAC characteristics (PA5 pin)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CCA}	Analog power supply	2.2	-	3.6	V	
V_{REF+}	Positive reference voltage	2.2	-	3.6	V	V_{REF+} ≤ V_{CCA}
V_{SSA}	Ground	0	-	0	V	
R_{LOAD}(1)	Load connected to V_{SSA}	5	-	-	kΩ	
	Load connected to V_{CCA}	15	-	-	kΩ	
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	The minimum resistive load between DAC_VOUT and V_{SS} to have a 1% accuracy is 1.5 MΩ when the buffer is OFF.
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (When the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{CCA}-0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5		mV	

Symbol	Parameter	Min	Typ	Max	Unit	Note
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-		V_{REF+} -10 mV	V	It gives the maximum output excursion of the DAC.
I_{CC_VREF+}	DAC DC V_{REF} current consumption in quiescent mode (Standby mode)	-		380	μA	With no load, worst code (0x0E4) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs.
I_{CCA}	DAC DC V_{CCA} current consumption in quiescent mode(2)	-		380	μA	With no load, middle code (0x800) on the inputs
		-		480	μA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(3)	Differential non linearity (Difference between two consecutive code-1LSB)	-	±3.5	-	LSB	Given for the DAC in 8-bit configuration
		-	±4		LSB	Given for the DAC in 12-bit configuration
INL(2)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	±3.5	-	LSB	Given for the DAC in 8-bit configuration
		-	±4	-	LSB	Given for the DAC in 12-bit configuration
Offset(2)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	±12	LSB	Given for the DAC in 12-bit configuration V_{REF+} = 3.3 V
		-	-	±3	LSB	Given for the DAC in 8-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(2)	Gain error	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}$(2)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	μs	C_{LOAD} ≤ 50pF, R_{LOAD} ≥ 5 kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	C_{LOAD} ≤ 50pF, R_{LOAD} ≥ 5 kΩ
t_{WAKEUP}(2)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	μs	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ input code between lowest and highest possible ones.
PSRR+(1)	Power supply rejection ratio (to V_{CCA}) (static DC measurement)	-	-67	-40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design, not tested in production.
2. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.

5.3.17. Temperature sensor characteristics

Table 5-31 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max(3)	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±2	±5	°C
Avg_Slope(1)	Average slope	2.0	2.2	2.4	mV/°C
V_{30}(1)	Voltage at 30℃	0.682	0.7	0.718	V
t_{START}(2)	Start up time	4	-	10	μs
T_{S_temp}(2)(3)	ADC sampling time when reading the temperature	20	-	-	μs

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. The shortest sampling time can be determined in the application by multiple iterations.

5.3.18. Embedded voltage reference characteristics

Table 5-32 Embedded voltage reference characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	1.17	1.2	1.23	V
$t_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	17.1	-	-	μs
V_{RERINT}	Internal reference voltage spread over the temperature range	-	-	10	mV
T_{Coeff}	Temperature coefficient of V_{REFINT}	-100	-	100	ppm/℃

1. Guaranteed by design, not tested in production.

5.3.19. Timer characteristics

Table 5-33 Timer characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 144 MHz	-	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 144 MHz	-	-	MHz
Res_{TIM}	Timer resolution time	-	-	16	bit
$t_{COUNTER}$	16-bit counter internal clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 144 MHz	-	-	μs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 144 MHz	-	-	s

Table 5-34 IWDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min	Max	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 5-35 WWDG characteristics (timeout period at 48 MHz PCLK)

Prescaler	WDGTB[1:0]	Min	Max	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

5.3.20. Communication interfaces

5.3.20.1. I²C interface characteristics

I²C interface meets the requirements of the I²C bus specification and user manual:

- Standard-mode (Sm): 100 kHz
- Fast-mode (Fm): 400 kHz

I²C SDA and SCL pins have analog filtering, see table below.

Table 5-36 I²C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter (Spikers shorter than the limiting duration are suppressed)	50	260	ns

The I²C timings requirements are specified by design when the I²C peripheral is properly configured. The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not true open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{CC} is disabled, but is still present.

Table 5-37 I²C filter characteristics

Symbol	Parameter	Standard I²C(1)		Fast I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4	-	0.6	-	µs
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ /$t_{r(SDL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ /$t_{f(SDL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4	-	0.6	-	
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF
t_{sp}	Pulse width of the spikes	0	50(4)	0	50(4)	µs

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 4 MHz to achieve standard mode I²C frequencies. f_{PCLK1} must be at least 8 MHz to achieve fast mode I²C frequencies.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The minimum width of the spikes filtered by the analog filter is above t_{SP}(max).

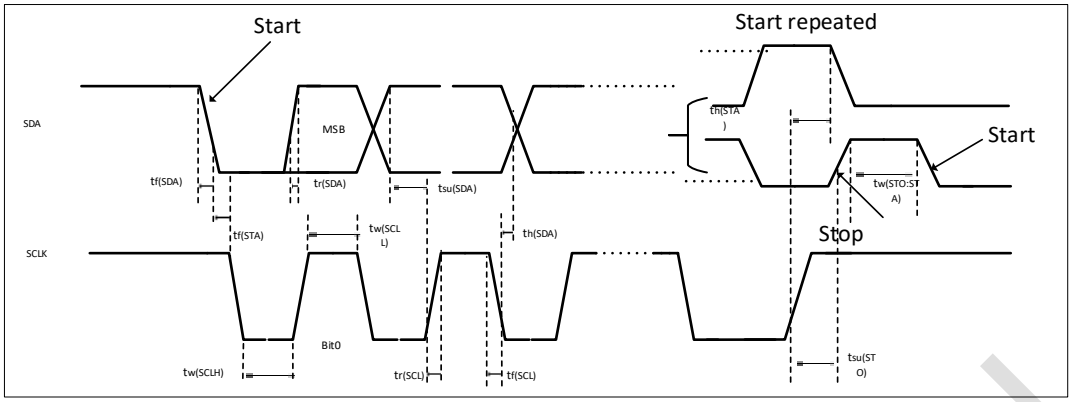


Figure 5-3 I²C bus timing diagram

5.3.20.2. SPI interface characteristics

Table 5-38 SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7 to 3.6 V	-	-	36	MHz
		Mater mode 1.8 to 3.6 V	-	-	36	
		Slave mode 2.7 to 3.6 V	-	-	36	
		Slave mode 1.8 to 3.6 V	-	-	36	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	-	5	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	-	55	%
$t_{su(NSS)}$	NSS setup time	Slave mode	$4*T_{pclk}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2\ T_{pclk}$	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high level/low level time	Master mode, presc = 4	$2*T_{pclk}-1$	$2*T_{pclk}$	$2*T_{pclk}+1$	
$t_{su(MI)}$	Data input setup time	Master mode, presc = 4	$T_{pclk}+4^{(1)}$	-	-	
$t_{su(SI)}$		Slave mode, presc = 4	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	-	
$t_{h(SI)}$		Slave mode	$T_{pclk}+4$	-	-	
$t_{a(SO)}$	Data output access time	Slave mode, presc = 4	0	-	$3*T_{pclk}$	
$t_{dis(SO)}$	Data output disable time	Slave mode	$2*T_{pclk}+5$	-	$4*T_{pclk}+5$	
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 to 3.6 V presc = 4	0	-	12 or $1.5*T_{pclk}$ (2)	
		Slave mode 1.8 to 3.6 V presc = 4	0	-	18 or $1.5*T_{pclk}$ (2)	
$t_{v(MO)}$		Master mode (after enable edge)	-	3.5	4.5	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge) presc = 4	0(3)	-	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	-	

1. The master generates a 1 PCLK receive control signal before the receive edge.
2. The slave has a maximum of 1 PCLK delay based on the SCK transmit edge, and defines 1.5 PCLK considering IO delay, etc.
3. The Slave updates the data before the transmit edge if the SCK duty cycle sent by the Master is wide between the receive edge and the transmit edge.

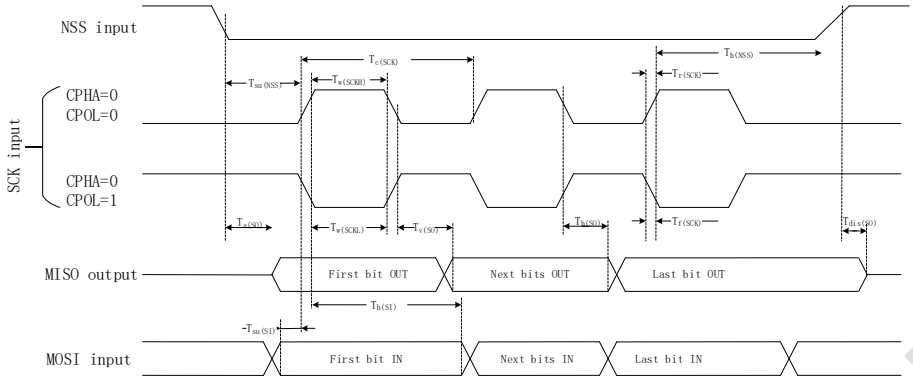


Figure 5-4 SPI timing diagram – slave mode and CPHA=0

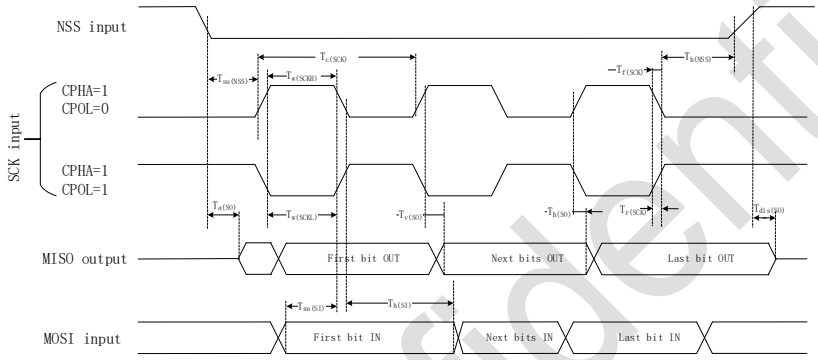


Figure 5-5 SPI timing diagram – slave mode and CPHA = 1(1)

1. Measurement points are done at CMOS level: 0.3 V_{CC} and 0.7 V_{CC}

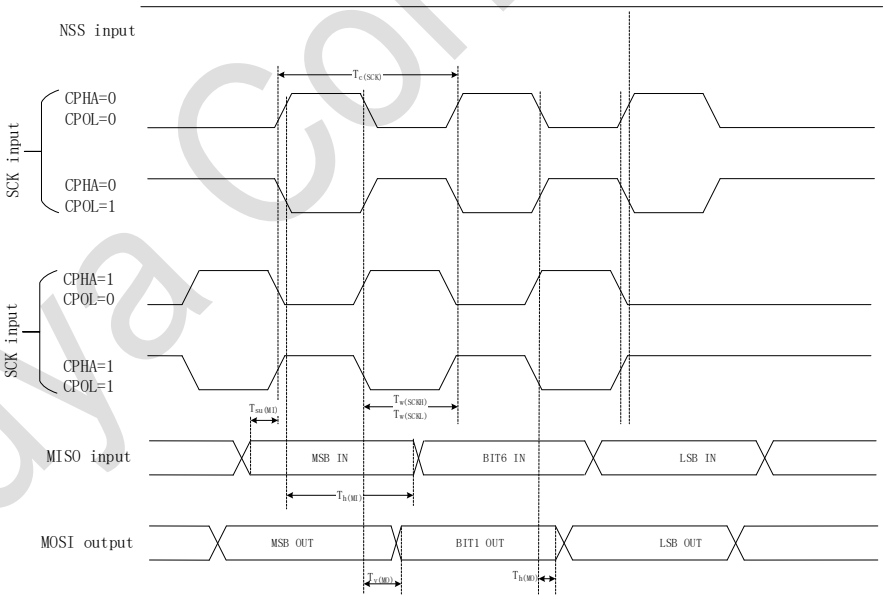


Figure 5-6 SPI timing diagram - slave mode(1)

1. Measurement points are done at CMOS level: 0.3 V_{CC} and 0.7 V_{CC}

5.3.20.3. I²S characteristics

Table 5-39 I²S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_S	I²S sampling frequency	-		8	192	kHz
f_{MCLK}	I²S main clock output	-		0.256 x f_s	0.256 x f_s	MHz
f_{CK} $1/t_{c(CK)}$	I²S clock frequency	Master data		-	0.064 x f_s	MHz
		Slave master		-	0.064 x f_s	
D_{CK}	I²S clock frequency duty cycle	Slave receiver		30	70	%
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load C_L = 50 pF		-	8	ns
$t_{v(WS)}$	WS valid time	Master mode			2	
$t_{h(WS)}$	WS hold time	Master mode		3	-	
		Slave mode		2	-	
$t_{su(WS)}$	WS setup time	Slave mode		4	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver		3	-	
$t_{su(SD\_SR)}$		Slave receiver		4	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver		5	-	
$t_{h(SD\_SR)}$		Slave receiver		2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave receiver (after enable edge)	2.7 to 3.6 V	-	15	
			1.8 to 3.6 V	-	22	
$t_{v(SD\_MT)}$		Master receiver (after enable edge)		-	2	
$t_{h(SD\_ST)}$	Data output hold time	Slave receiver (after enable edge)		7	-	
$t_{h(SD\_MT)}$		Master receiver (after enable edge)		1	-	

1. The maximum value of 256xFs is not exceeding 49.152 MHz.

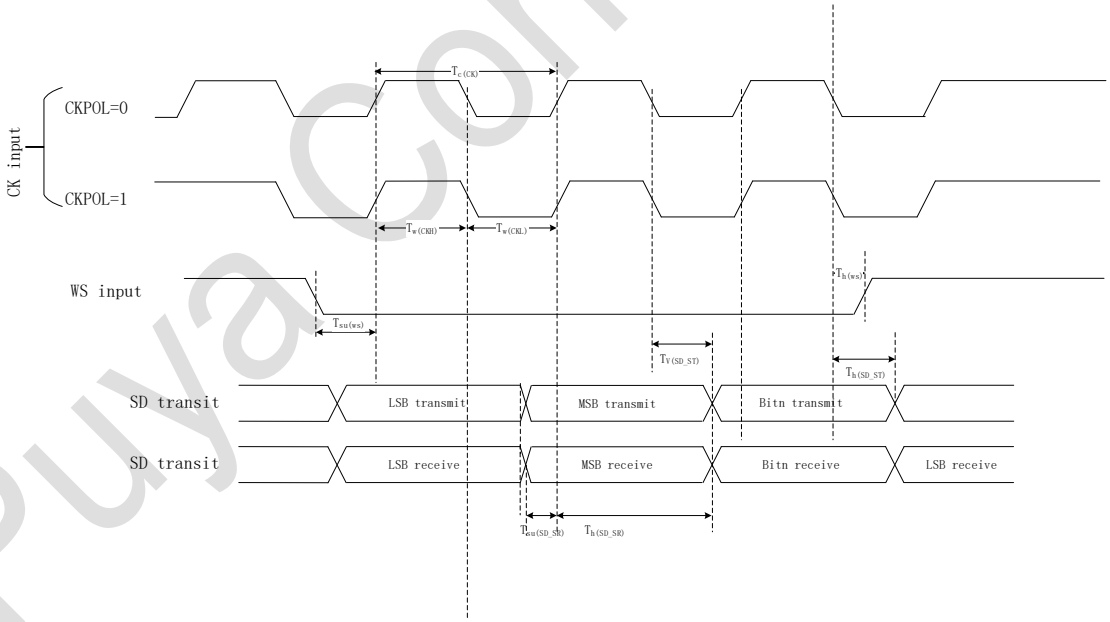


Figure 5-7 I²S slave timing diagram (Philips protocol)

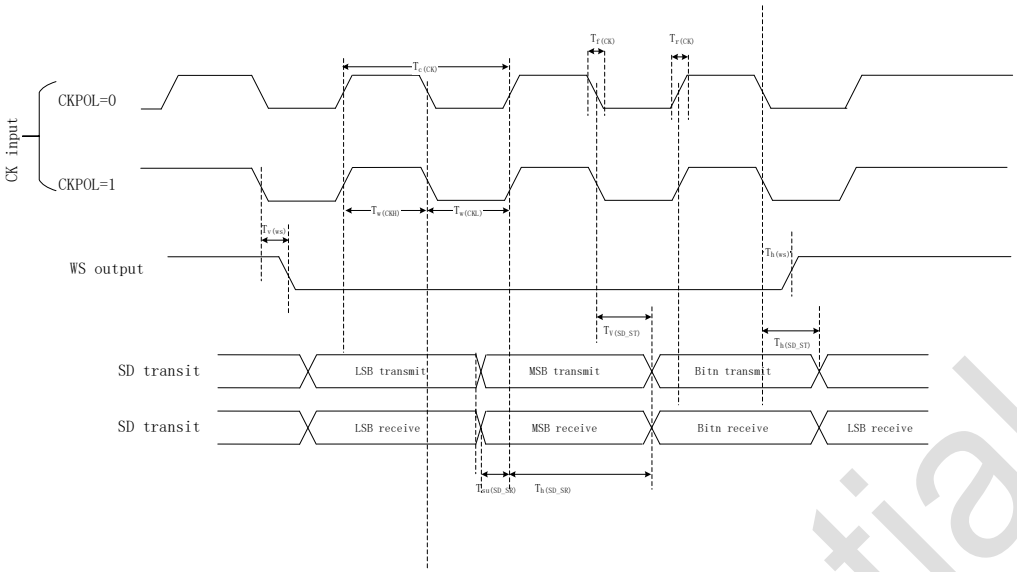


Figure 5-8 I²S master timing diagram (Philips protocol)

5.3.20.4. USB characteristics

Table 5-40 USB startup time

Symbol	Parameter	Max	Unit
t_{START}(1)	USB transceiver startup time	1	μs

1. Guaranteed by design, not tested in production.

Table 5-41 USB DC electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
V_{CC}	USB transceiver operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(3)	Differential input sensitivity	I (USB_DP, USB_DM)	0.2	-	
V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(3)	Single ended receiver threshold	-	1.3	2	
Output voltage					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. The USB transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics, which are degraded in the 2.7 to 3.0 V V_{CC} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB drivers.

Table 5-42 USB OTG full speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(2)	C_L <= 50 pF	4	20	ns
t_f	Fall time(2)	C_L <= 50 pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal.

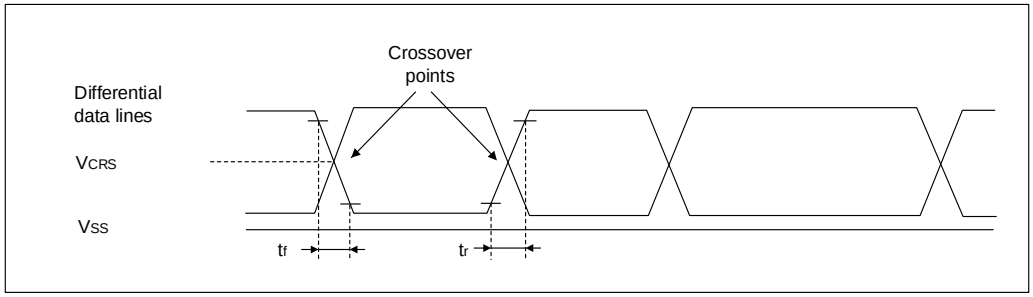


Figure 5-9 USB timing: data signal rise and fall time definition

5.3.20.5. SD/SDIO MMC card host interface (SDIO) characteristics

Table 5-43 SD/MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	C_L = 30 pF	0	48	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} = 48 MHz	8.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 48 MHz	8.3	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode					
t_{ISU}	Input setup time	f_{PP} = 48 MHz	3.5	-	ns
t_{IH}	Input hold time	f_{PP} = 48 MHz	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	f_{PP} = 48 MHz	-	7	ns
t_{OH}	Output hold time	f_{PP} = 48 MHz	3	-	
CMD, D inputs (referenced to CK) in SD default mode					
t_{ISUD}	Input setup time	f_{PP} = 24 MHz	1.5	-	ns
t_{IHD}	Input hold time	f_{PP} = 24 MHz	0.5	-	
CMD, D outputs (referenced to CK) in SD default mode					
t_{OVD}	Output valid default time	f_{PP} = 24 MHz	-	6.5	ns
t_{OHD}	Output hold default time	f_{PP} = 24 MHz	3.5	-	

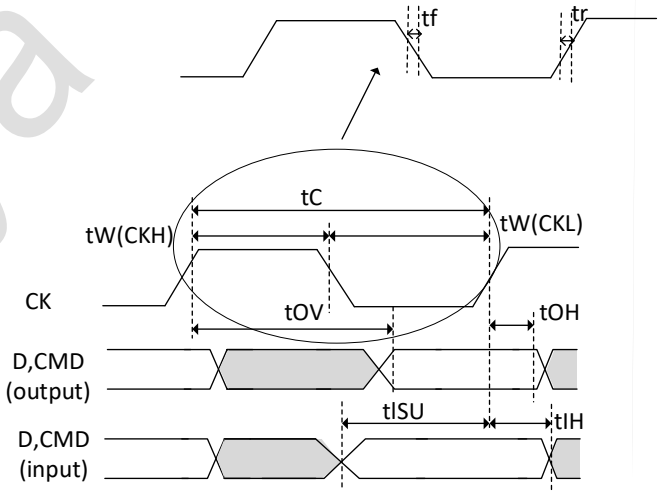


Figure 5-10 SDIO high-speed mode

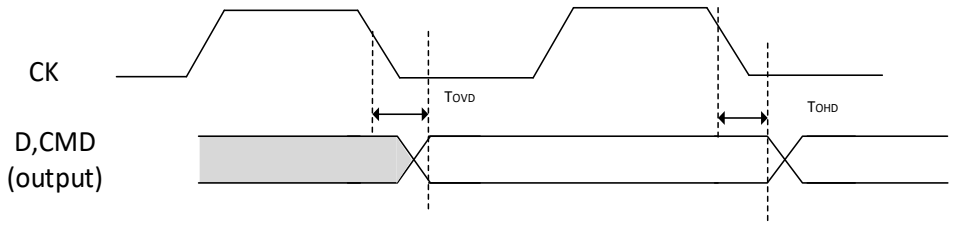


Figure 5-11 SDIO default mode

5.3.20.6. ESMC characteristics

Table 5-44 ESMC characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{QCK}	Clock frequency	1.8 < V_{CC} < 3.6 V	-	-	24	MHz
$t_{w(CKH)}$	Clock high level/low level time	1.8 < V_{CC} < 3.6 V	t_{QCK}/2-0.5	-	t_{QCK}/2+1	ns
$t_{w(CKL)}$			t_{QCK}/2-1	-	t_{QCK}/2+0.5	
$t_{s(IN)}$	Data input setup time	1.8 < V_{CC} < 3.6 V	1	-	-	
$t_{h(IN)}$	Data input hold time	1.8 < V_{CC} < 3.6 V	5	-	-	
$t_{v(OUT)}$	Data output valid time	1.8 < V_{CC} < 3.6 V	-	1	1.5	
$t_{h(OUT)}$	Data output hold time	1.8 < V_{CC} < 3.6 V	0.5	-	-	

1. Evaluated by characterization, not tested in production.
2. This parameter is tested in both single-wire and dual-wire modes. The maximum frequency is 18 MHz in both quad-wire and dual-quad-wire modes.

Table 5-45 ESMC characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CKH)}$	Clock high level/low level time	1.8 < V_{CC} < 3.6 V	t_{QCK}/2	-	t_{QCK}/2+1	ns
$t_{w(CKL)}$			t_{QCK}/2-1	-	$t_{QCK/2}$+0.5	
$t_{sr(IN)}$	Data input setup time (rising edge)	1.8 < V_{CC} < 3.6 V	2	-	-	
$t_{sf(IN)}$	Data input setup time (falling edge)	1.8 < V_{CC} < 3.6 V	2	-	-	
$t_{hr(IN)}$	Data input hold time (rising edge)	1.8 < V_{CC} < 3.6 V	5	-	-	
$t_{hf(IN)}$	Data input hold time (falling edge)	1.8 < V_{CC} < 3.6 V	5	-	-	
$t_{vr(OUT)}$	Data output valid time (falling edge)	1.8 < V_{CC} < 3.6 V	-	-	9	
$t_{vf(OUT)}$	Data output valid time (rising edge)	1.8 < V_{CC} < 3.6 V	-	-	11	
$t_{hr(OUT)}$	Data output hold time (rising edge)	1.8 < V_{CC} < 3.6 V	2	-	-	
$t_{hf(OUT)}$	Data output hold time (falling edge)	1.8 < V_{CC} < 3.6 V	3	-	-	

1. Evaluated by characterization, not tested in production.

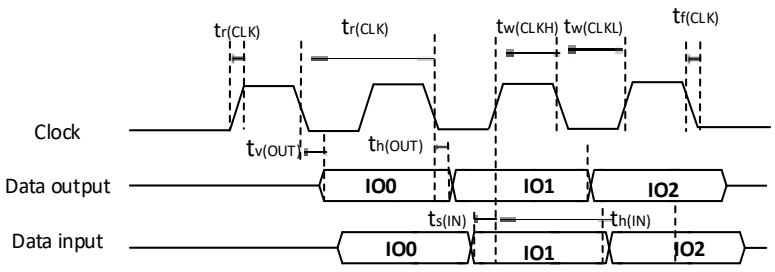


Figure 5-12 ESMC timing diagram-SDR Mode

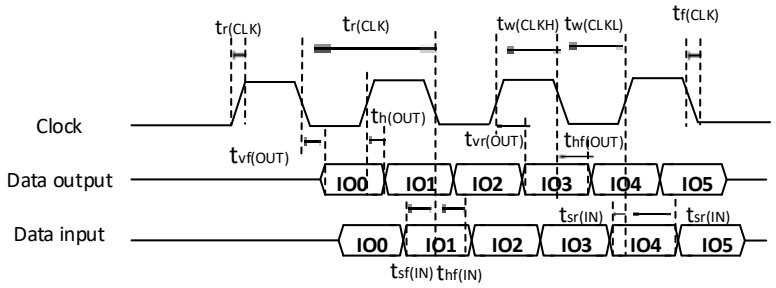


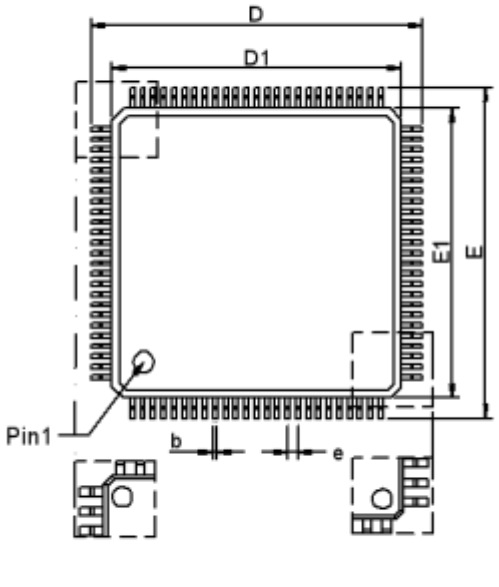
Figure 5-13 ESMC timing diagram-DDR Mode

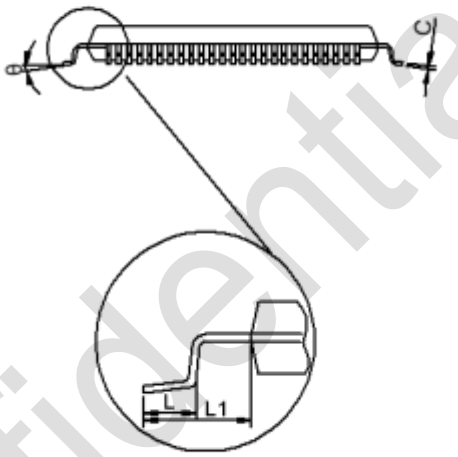
5.3.20.7. CANFD interface characteristics

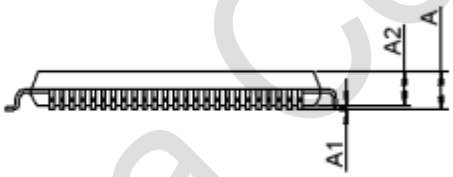
Refer to Section 5.3.14: I/O port characteristics for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

6. Package information

6.1. LQFP100 package size







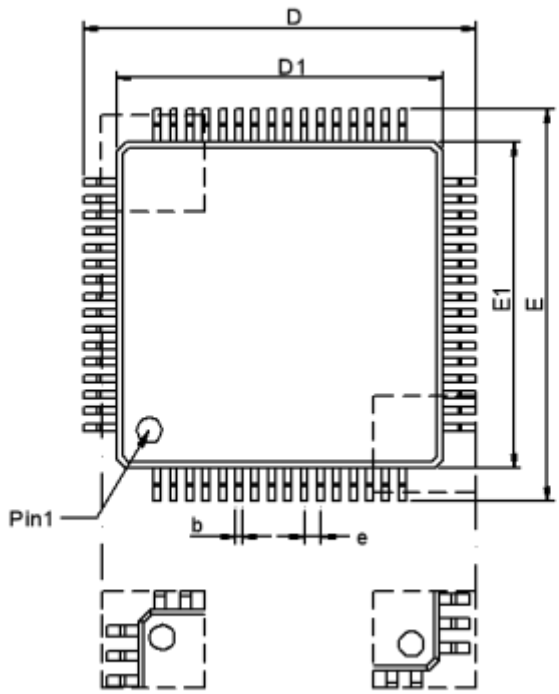
Common Dimensions
(Unit of Measure=millimeters)

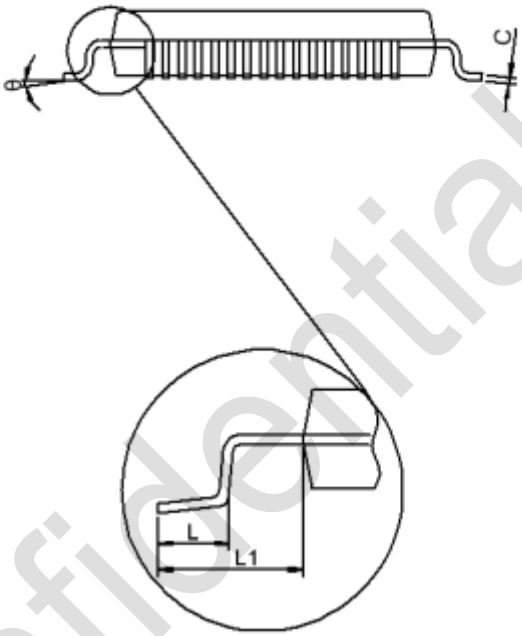
Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	15.800	16.000	16.200
D1	13.900	14.000	14.100
E	15.800	16.000	16.200
E1	13.900	14.000	14.100
e		0.500BSC	
L	0.450	-	0.750
L1		1.000REF	
θ	0	-	7°

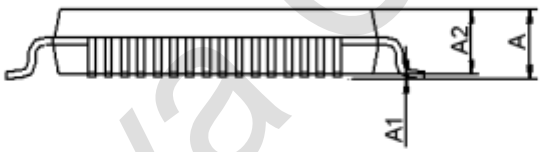
Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP100L 14x14X1.4-0.5PITCH	QRPD-0052	1.1

6.2. LQFP64 package size







Common Dimensions

(Unit of Measure=millimeters)

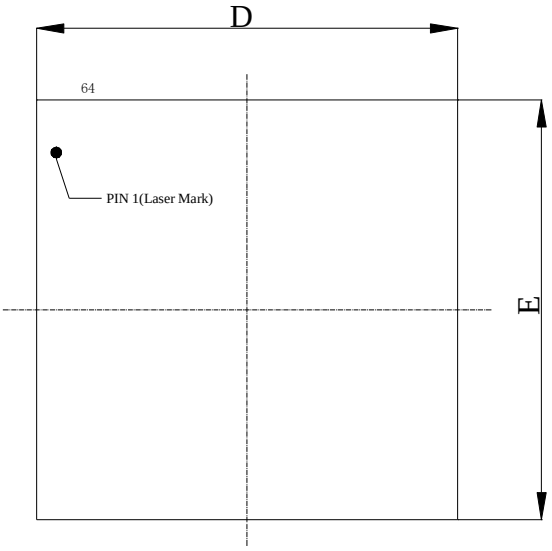
Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	11.950	12.000	12.050
D1	9.900	10.000	10.100
E	11.950	12.000	12.050
E1	9.900	10.000	10.100
e		0.500BSC	
L	0.530	-	0.700
L1		1.000REF	
θ	0	-	7°

Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

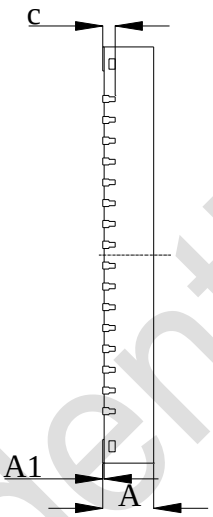
	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP64L 10x10X1.4-0.5PITCH	QRPD-0051	1.1

6.3. QFN64 package size

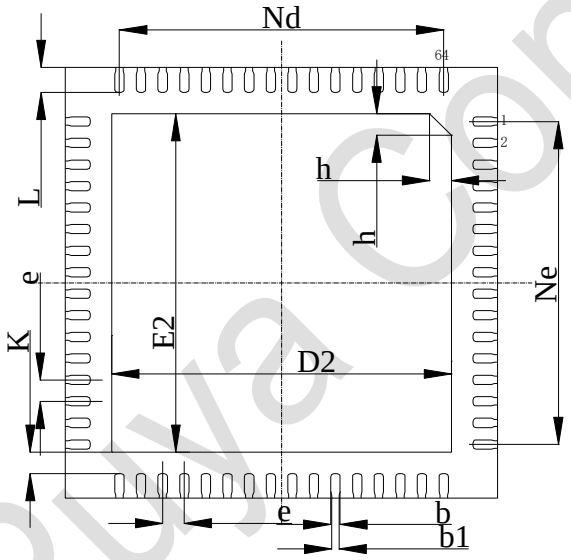
TOP VIEW



SIDE VIEW



BOTTOM VIEW



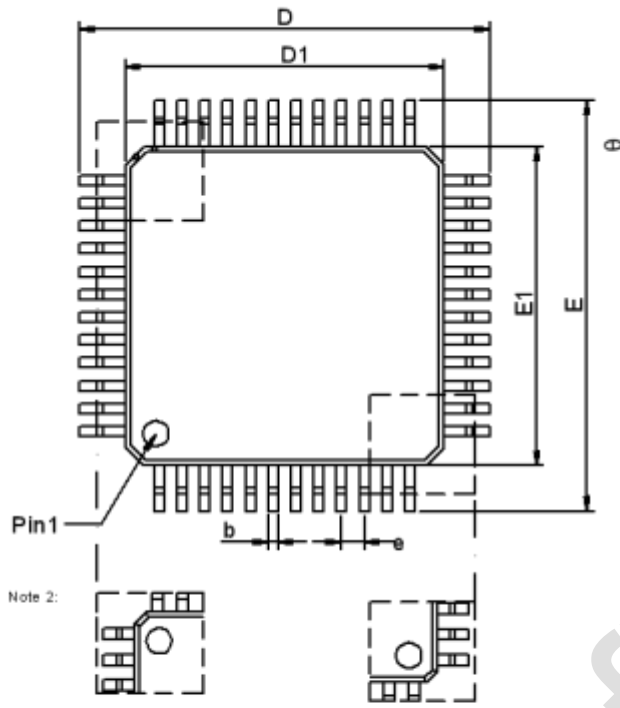
Common Dimensions

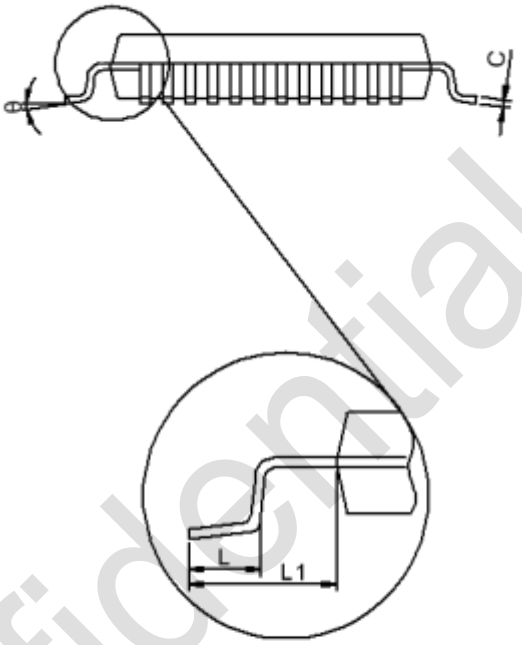
(Unit of Measure=millimeters)

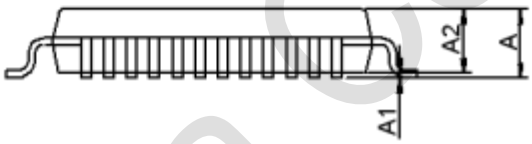
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.10	0.15	0.20
b1	0.12REF		
c	0.203REF		
D	6.90	7.00	7.10
D2	5.40	5.50	5.6
e	0.35BSC		
Ne	5.25BSC		
Nd	5.25BSC		
E	6.90	7.00	7.10
E2	5.40	5.50	5.60
L	0.35	0.40	0.45
K	0.35REF		
h	0.30	0.35	0.40

	TITLE	DRAWING NO.	REV
PUYA	PUYA QFN64 7X7X0.75-0.35PITCH POD_V1.0	QRPD-0097	V1.0

6.4. LQFP48 package size







Common Dimensions
(Unit of Measure=millimeters)

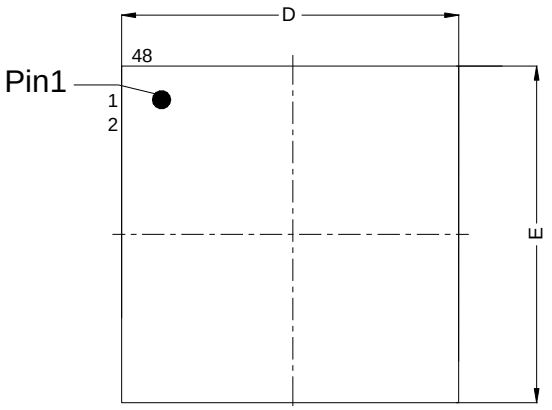
Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	8.800	9.000	9.200
D1	6.900	7.000	7.100
E	8.800	9.000	9.200
E1	6.900	7.000	7.100
e		0.500BSC	
L	0.450	-	0.750
L1		1.000REF	
θ	0	-	7°

Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

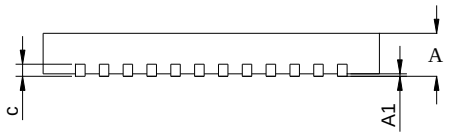
	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP48L 7x7X1.4-0.5PITCH	QRPD-0050	1.1

6.5. QFN48 package size

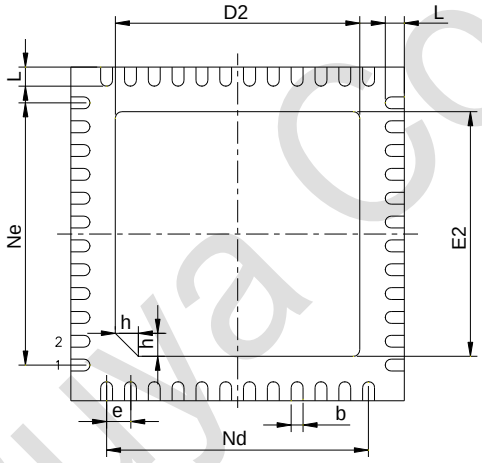
TOP VIEW



SIDE VIEW



BOTTOM VIEW



Common Dimensions
(Unit of Measure=millimeters)

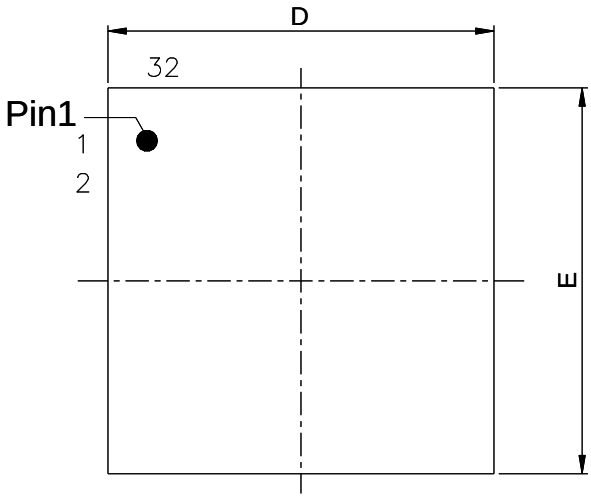
Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c		0.200REF	
D	5.900	6.000	6.100
D2	4.100	4.300	4.500
E	5.900	6.000	6.100
E2	4.100	4.300	4.500
e		0.400BSC	
Nd		4.400BSC	
Ne		4.400BSC	
L	0.300	0.400	0.500
h	0.300	0.350	0.400

Note：1. Dimensions are not to scale

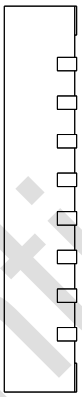
	TITLE	DRAWING NO.	REV
PUYA	Puya QFN48L 6X6X0.75-0.4PITCH POD	QRPD-0056	1.1

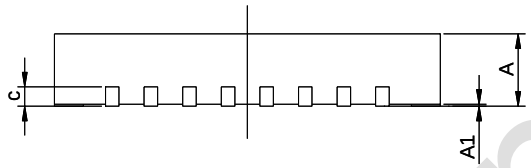
6.6. QFN32 (4*4) package size

TOP VIEW

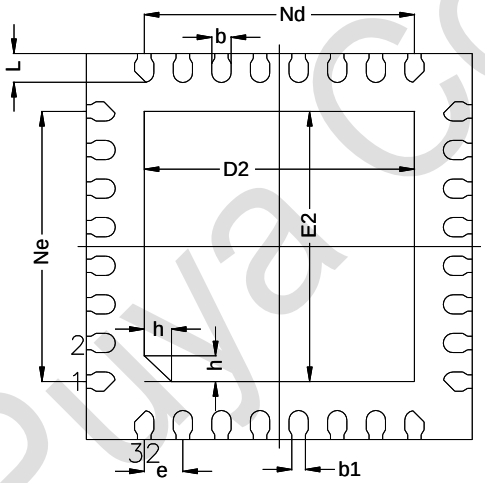


SIDE VIEW





BOTTOM VIEW



Common Dimensions

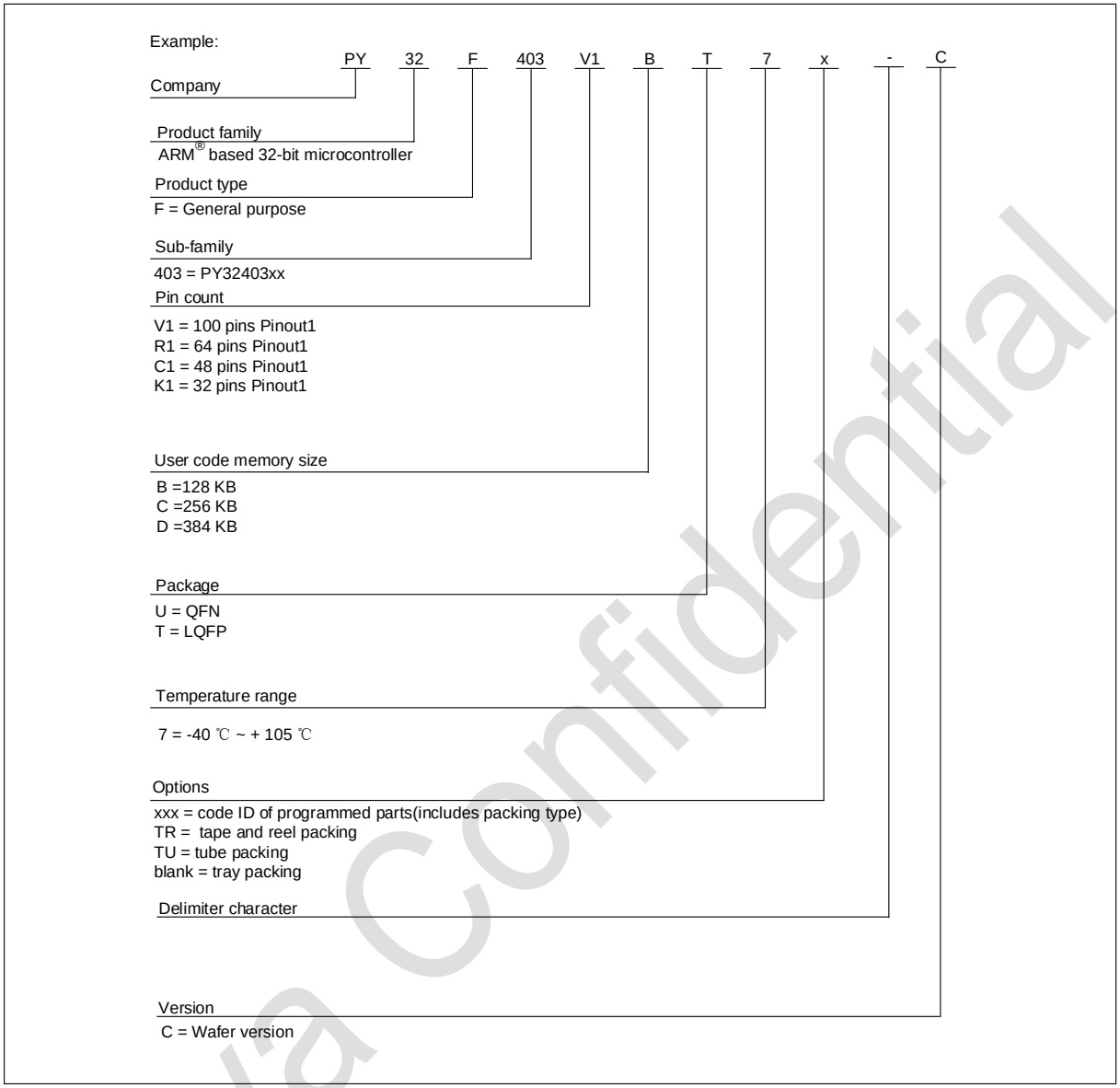
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.650	2.850	3.050
E	3.900	4.000	4.100
E2	2.650	2.850	3.050
e	0.400BSC		
Nd	2.800BSC		
Ne	2.800BSC		
b1	0.140REF		
L	0.200	0.300	0.400
h	0.300	0.350	0.400

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN32L 4X4X0.75-0.4PITCH POD	QRPD-0060	1.2

7. Ordering information



8. Version history

Version	Date	Descriptions
V0.2	2025.06.20	Initial version
V0.3	2025.07.14	Add product PY32F403K1CU7-C
V0.4	2025.10.10	Add product PY32F403C1CT7-C, PY32F403R1DT7-C and PY32F403R1DU7-C
V0.5	2026.1.9	1. Add product PY32F403C1DT7-C 2. Modify table 5-16 and 5-17

Puya Semiconductor Co., Ltd.